QUANTEL

DIGITAL CEL RECORDER
DCR 7700/1 HARRY
INSTALLATION AND SERVICE MANUAL

Harry™

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THIS MANUAL IS REVISION "C".

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RFI Statement

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the service manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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SECTION 1 : GENERAL

1:1:1 Introduction

Harry is a broadcast Digital Cel Recording system, which processes broadcast specification video. This allows a moving television picture sequence to be stored, processed and replayed without degradation. The digital video information stored can be edited and mixed to produce loss free multiple generation sequences.

The Digital Cel Recorder is a "Real Time" system, which can record live pictures, process and edit them, then replay them at video rate. Harry provides full Match Frame editing facilities by using Time coding techniques. Harry is designed to be completely compatible with the Quantel DPB 7000 Paintbox series, which provide the facility of full Frame cel animation.

The Harry system, when connected to the DPB 7000 series Paintbox, can be used to produce full frame cel animation sequences, which can be freely mixed with stored video to produce a wide range of animation effects. The connection of Paintbox to the Harry system also allows recorded video clips to be modified frame by frame using the Paintbox.

The DPE 5800/1 Encore production effects system can be easily connected to the Harry system digital Input and Output to allow processing of stored Cels and clips, without repeated conversion between Analogue and Digital video.

The Harry system is capable of accepting Coded, R.G.B. and Y.U.V. analogue input video sources, which are digitally decoded and coded within the system to SMPTE/CCIR recommendations (rec 601).

The Harry system is controlled via a powerful Menu display and user control station consisting of a Digitized Tablet, a Pressure sensitive Pen and a Keyboard.

All user and Engineering functions are "soft" and controlled via the menu display, and stored in "non volatile" memory within the system. A number of Engineering set-ups can be stored thus providing for the needs of various different studios. These setups can be recalled as required using the menu display.

1:1:2 Auxiliary Equipment

(a) A VDU/Terminal may be required for some service purposes.

(b) The Operator station will require a Colour monitor connected to the Harry unit Main Output.

1:1:3 Installation and Service Manual

(a) GENERAL

This manual only contains information relevant to the installation, service and maintenance of the Harry system. This manual does not contain information relating to the operation of the Harry system.

(b) MANUAL REVISION STATUS

This Manual is a change controlled document and is related directly to the status of the Printed Circuit Boards within the system. Each section of this manual is given an issue letter which represents the status of the section. The PCB artwork issues determine the issue of the sections which relate directly to a specific PCB.

The contents list of this Manual gives issue details for each section within the manual. The issue reference for each section is printed in round brackets in the top right hand corner of each page. The first number determines which Chapter, the second number determines which section and the letter determines the issue of the section.

The issues of all sections in the manual determines the revision status of the manual, therefore any changes to any section in the manual raises the revision status of the manual.

Always quote the revision status and type number of the manual and the machines serial number when re-ordering this manual.

(c) CONTENT

Chapter 1 provides the system's broadcast video, physical and environmental specifications.

Chapter 2 is an installation guide, giving installation instructions, which cover environment, rack mounting, cabling and system interfacing

Chapter 3 gives full details of the system's built in diagnostics facilities, a description of the complete system, and maintenance instructions. This chapter also includes internal interconnection and connector details.

Chapter 4 provides circuit diagrams, block diagrams, component layouts and circuit descriptions for each of the front mounted printed circuit boards in the Harry unit.

Chapter 5 provides circuit diagrams, component layouts and circuit descriptions for each of the system's printed circuit boards not mounted in the front of the unit.

SECTION 2 : EQUIPMENT SPECIFICATION

(1,2A)

1:2:1 **Digital Coding System**

The digital coding system used by the Digital Cel Recording system conforms to the international recommendations of SMPTE and CCIR for Digital video processing:

(a) Y : component sampled at 13.5MHz, 8 bits, black = 16 and white = 235

(b) B-Y : component sampled at 6.75MHz, 8 bits, zero = 128 and range = 224

(c) R-Y : component sampled at 6.75MHz, 8 bits, zero = 128 and range = 224

(d) RGB/YUV inputs are coded appropriately.

(e) Digital inputs and outputs are compatible with these recommendations.

1:2:2 **Mainframe Connections** (see chapter 3 for cable details)

(a) Video signal connectors are of the BNC type 75 ohms.

(b) Digital video connectors are male 50 way ID ribbon type.

(c) Control connections are female 9 way D-type.

(d) Power connectors are 20 Amp IEC.

(e) Disc Data connectors are male 50 way ID ribbon type.

(f) Time Code connections is a 3-pin "X series" audio connector.

1:2:3 **Control Link**

(a) Data transmission is via an RS 422 link.

(b) Data transmission rate is 9600 baud.

(c) Maximum recommended cable length 300 metres.

(d) Cable is screened 4-way.

1:2:4 **Coded Input Video Specification**

(a) Composite coded colour signal 625/50 PAL or 525/60 NTSC.

(b) 1 volt pk-pk video. 100% saturation 700mv PAL or 714mv with setup NTSC.

(c) Input impedance 75 ohm. Return loss better than -30dB.

(d) Sync and burst locking level +&- 6dB.

1:2:5 Locking Reference Specification

(a) Black and burst or clean composite signal.

(b) High impedance loop through. Return loss better than -30dB.

1:2:6 RGB Input Specification

(a) Inputs 700mv PAL, 714mv NTSC into 75 ohms

Note: The RGB inputs are clamped during blanking, therefore the RGB input signals should have no unwanted level changes during line blanking.

1:2:7 YUV Input Specification

(a) Y = 700mv PAL, 714mv NTSC into 75 ohms.

(b) U and V (100% Saturated) = 700mV pk-pk into 75 ohms.

1:2:8 Coded Output Video Specification (Coded input/output)

(a) 1 volt into 75 ohms.

(b) Frequency response flat within +/- 0.3dB to 5.5MHz (PAL) 5MHz (NTSC).

(c) Field tilt (100% Flat Field)	<1%.
(d) Line tilt (100% Flat Field)	<1%.
(e) 2T pulse to bar amplitude	<2%.
(f) 2T K factor ringing	<2%.
(g) Chrominance/luminance gain inequality	<2%.
(h) Chrominance/luminance delay inequality	<+/-10ns.
(i) Differential Phase (analogue)	3°.
(j) Differential Gain (analogue)	4%.
(k) Vector accuracy 100% vector amplitude	<3% 3°.
(l) Signal/noise ratio 10KHz - 5.5MHz (PAL) - 5MHz (NTSC)	
i. Un-weighted including quantising errors	>50dB.
ii. Un-weighted neglecting quantising errors	>60dB.

1:2:9 **RGB Output Video Specification** (RGB input/output)

(a) 100% saturation 700mv (PAL), 714mv (NTSC) into 75 ohms.	
(b) Frequency response flat within +/- 0.3dB to 5MHz.	
(c) Field tilt (100% Flat Field)	<1%.
(d) Line tilt (100% Flat Field)	<1%.
(e) 2T pulse to bar amplitude	<2%.
(f) 2T K factor ringing	<2%.

1:2:10 **YUV Output Video Specification** (YUV input/output)

(a) Y = 700mv PAL, 714mv NTSC into 75 ohms	
(b) U and V (100% Saturated) = 700mV pk-pk into 75 ohms	
(c) Y Field tilt (100% Flat Field)	<1%.
(d) Y Line tilt (100% Flat Field)	<1%.
(e) Y 2T pulse to bar amplitude	<2%.
(f) Y 2T K factor ringing	<2%.

1:2:11 **Physical Dimensions**

	Height	**Depth**	**Width**	**Weight**
Mainframe	844mm	670mm	19 inch	65Kg
Disc Drive	356mm	766mm	19 inch	95Kg
TDS Tablet	15-60mm	420mm	550mm	7Kg

1:2:12 **Power Consumption**

(a) Mainframe 1.8KVA +/- 10%;
PAL 240 volts (+/- 10%) 50 Hz (+/-2%)
NTSC 110 volts (+/- 10%) 60 Hz (+/-2%)

(b) Disc Drive 1.0kVA +/- 10%;
PAL 240 volts (+/- 10%) 50 Hz (+/-2%)
NTSC 110 volts (+/- 10%) 60 Hz (+/-2%)

(c) Control System 100VA +/- 10%;
240 volts (+/- 10%) 50 Hz (+/-2%)
220 volts (+/- 10%) 50 Hz (+/-2%)
115 volts (+/- 10%) 60 Hz (+/-2%)

1:2:13 Operating and Storage Environment

Before powering up each unit of the system the unit must be given at least 3 hours to acclimatize to the environment in which the system is to be used. Powering up the system before the equipment has time to acclimatize may cause damage due to condensation.

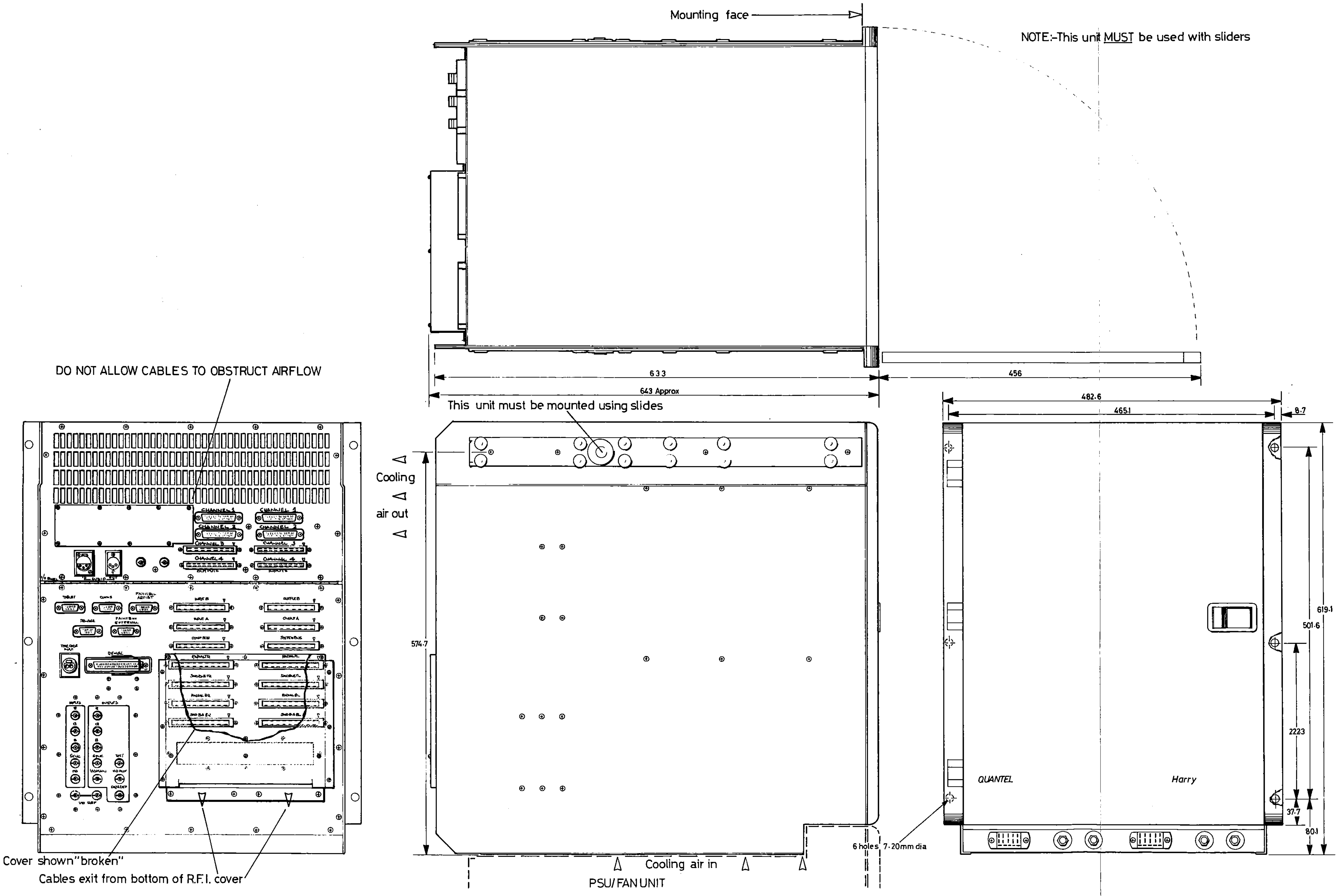
When the equipment is stored for a prolonged period, avoid locations where the environment is extreme. Equipment should be stored properly packed. When the temperature difference between shipping (or storage) exceeds 20^{o}C, the equipment should be allowed to remain packaged for more than 3 hours to avoid condensation when unpacking.

(a) operating temperature range 10 to 35^{o}C

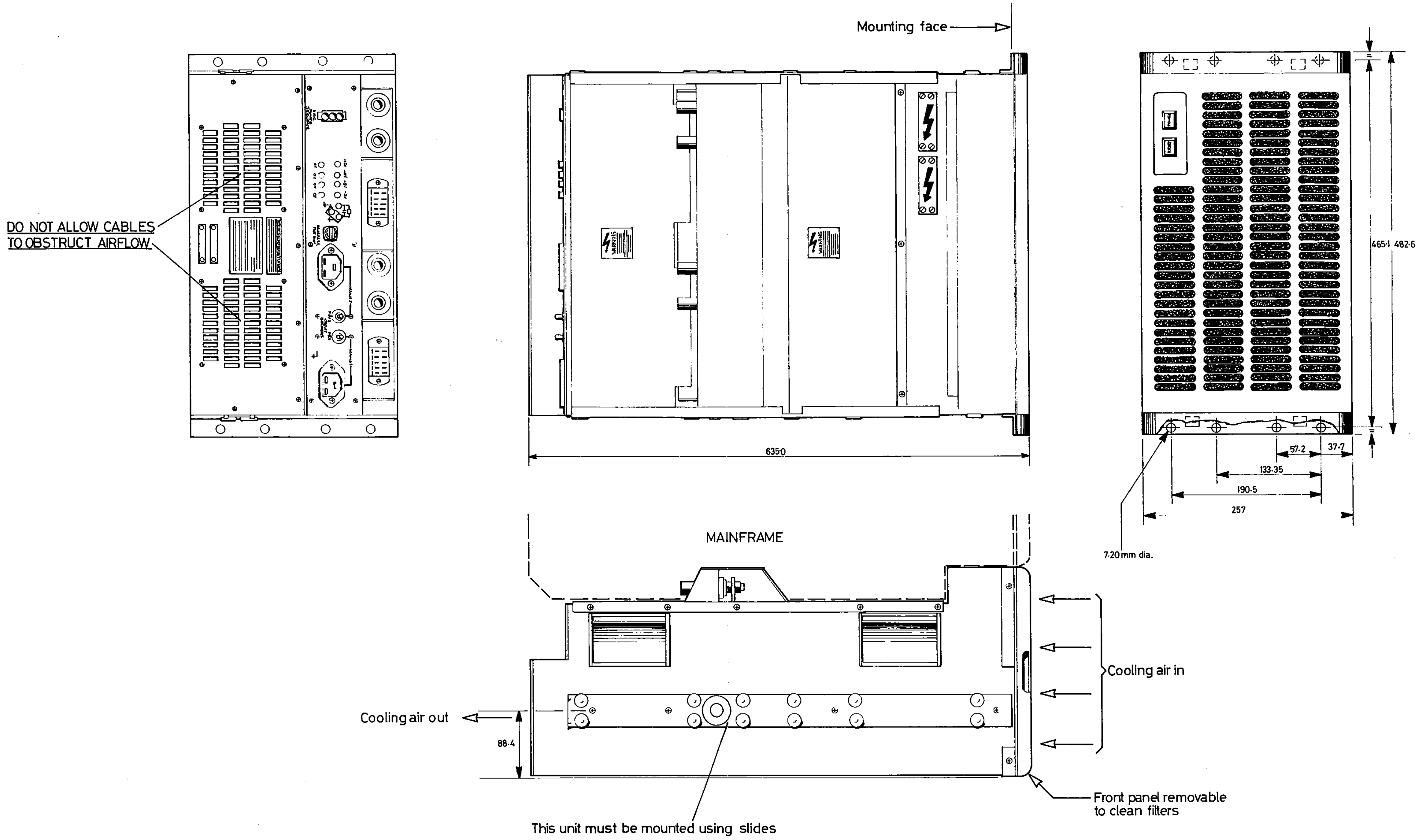
(b) Storage temperature range -5 to +60^{o}C

(c) Humidity non-condensing 20% to 80% RH

FIGURE 1.3.1 CRATE ASSEMBLY DATA



(1,3A)
FIGURE 1.3.2 PSU ASSEMBLY DATA


DO NOT ALLOW CABLES TO OBSTRUCT AIRFLOW
Mounting face
635·0
465·1
482·6
57·2
37·7
133·35
190·5
257
7·20mm dia.
MAINFRAME
Cooling air in
Cooling air out
88·4
Front panel removable to clean filters
This unit must be mounted using slides

(1,3A)
FIGURE 1.3.3 TDS TABLET DATA

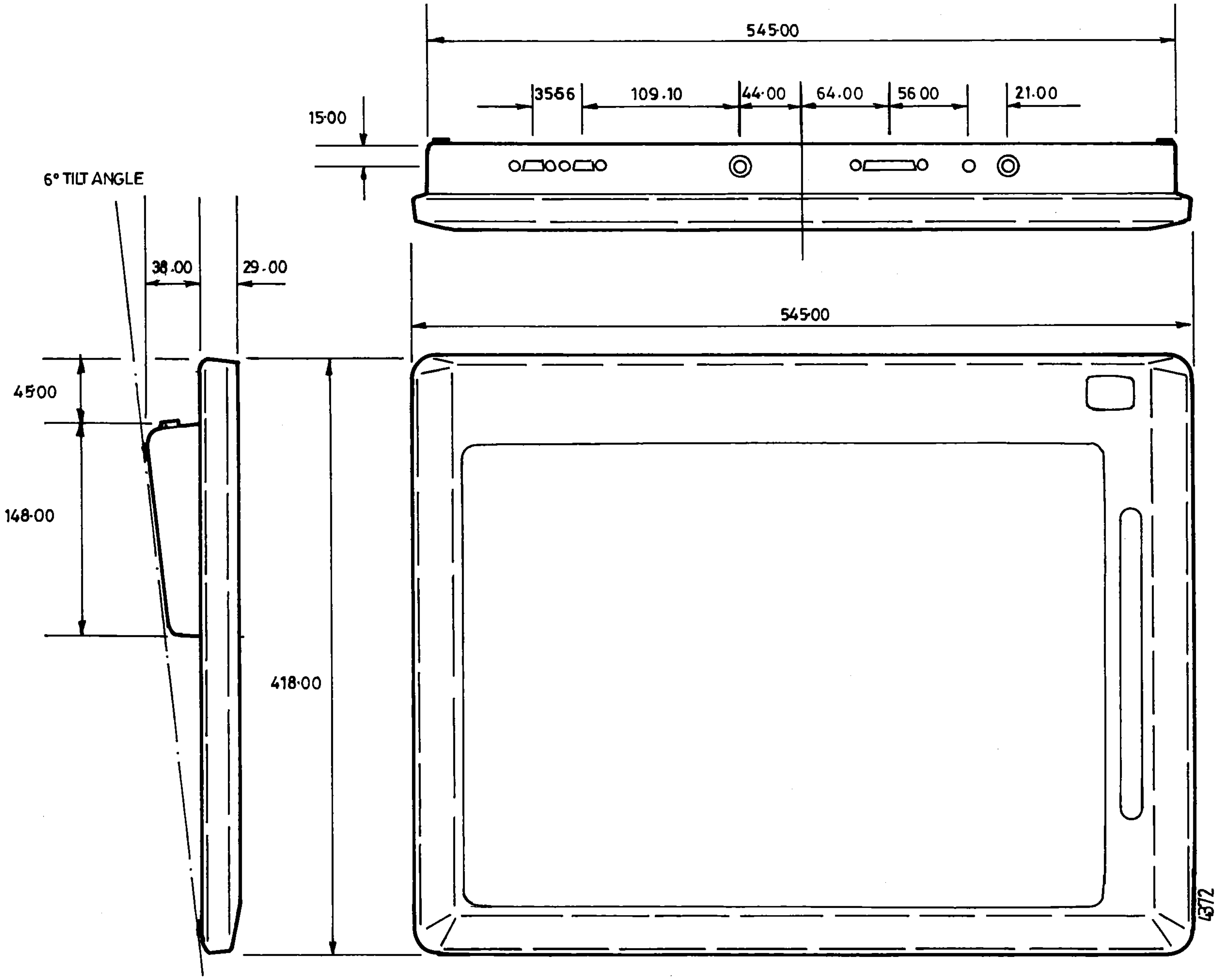
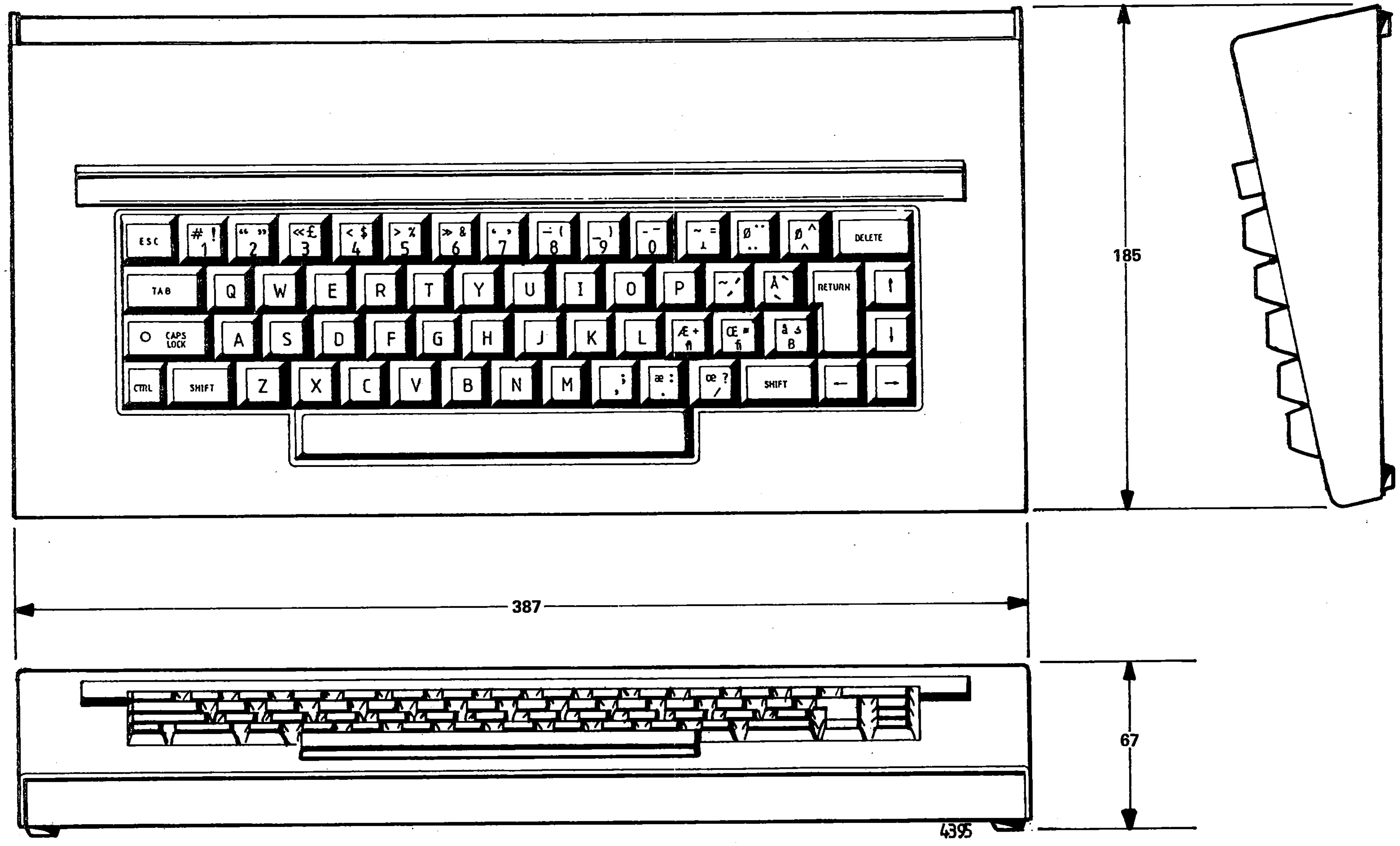


FIGURE 1.3.4 KEYBOARD DATA



DCR 7700/1 HARRY
INSTALLATION AND SERVICE MANUAL
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SECTION 1 : GENERAL

2:1:1 Introduction

This chapter contains information relevant to the unpacking, rack mounting and alignment of the Harry system ready for operation. PLEASE READ this chapter before installing the system, as the instructions contained have been produced to make the process of installation as simple as possible, and to ensure that the system remains reliable.

As a complex system of electronic hardware, Harry must be correctly installed with the physical and environmental considerations explained in this chapter adhered to.

QUANTEL Ltd can take no responsibility for equipment failure due to incorrect installation.

Note: When the equipment is stored for a prolonged period, avoid locations where the environment is extreme. Equipment should be stored properly packed. When the temperature difference between shipping (or storage) exceeds 20°C, the equipment should be allowed to remain packaged for more than 3 hours to avoid condensation when unpacking.

2:1:2 Before Installing Equipment

It is advisable, when rack mounting the Harry system, to have available a Fork-Lift as each unit within the system weighs approximately 90 Kg. A number of units in the system will have to be lifted and rack mounted above waist height.

If the Harry system is to be used with other equipment, ensure that any special requirements have been fulfilled.

SECTION 2 : ENVIRONMENTAL CONDITIONS

2:2:1 General

The Harry system is a complex electronics device and care should be taken in the choice of installation environment to ensure peak performance and reliability. The following points should be remembered when installing the Harry system, to minimize possible failure:

(a) Avoid exposure to direct sunlight or any other strong direct lights.

(b) Avoid areas subject to vibration and areas where dust contamination is possible.

(c) Avoid installations near sources of direct heat.

(d) Ensure that the ambient air temperature is kept within the range 10°C - 35°C. Note: the system contains over temperature circuitry, which is calibrated with an ambient air temperature of 30°C.

(e) Ensure that good air circulation around the rack is provided to prevent heat build up. Air holes should be given adequate clearance. Ensure that no ventilation holes on the Harry crate assembly or the Disc Drive units are restricted, because over heating will occur.

(f) Ensure that power, data and signal cables are not run together and that they are tied back to avoid obstructing the air flow.

(g) Ensure that the floor where the Harry system is to be located can withstand the total system weight. Do not install the Harry system in racks mounted on wheels.

(h) Ensure adequate space is left at the front and rear of the Rack Mounted system, so that access is possible to the crate mounted electronics.

It is recommended that the Harry system is connected to a "Technical Electrical Supply"; free from interference and L.F. transients etc. Note that the quality of electrical supply will affect the reliability of some system components.

2:2:2 Equipment Location

The Harry crate assembly and the Disc drive units should be rack mounted as described in this chapter. The cabling should be carried out using the shortest possible lengths, to avoid interference from stray Electro-magnetic fields.

The DPB 7000/1 Paintbox crate assembly should be rack mounted as part of the Harry system to avoid corrupted data transfer caused by long cable lengths. The Tablet and controller can be situated up to 300 Metres from the system as the connection is via an RS 422 serial link.

2:2:3 System Air Flow

The air flow through the units in the Harry system is complex and the cabinets, which are to hold the system, must be located carefully to ensure adequate clearance to provide for the correct cooling of the system.

If the system is operated in a confined area, additional external cooling may be required.

Ensure that the hot air expelled from one unit is not drawn into another as this may cause the unit to overheat and subsequently cause damage.

(a) HARRY AIR FLOW

The Harry crate assembly and PSU cools front to back; that is cool air is drawn through the front of the Power supply unit and hot air is blown out at the rear of the crate assembly.

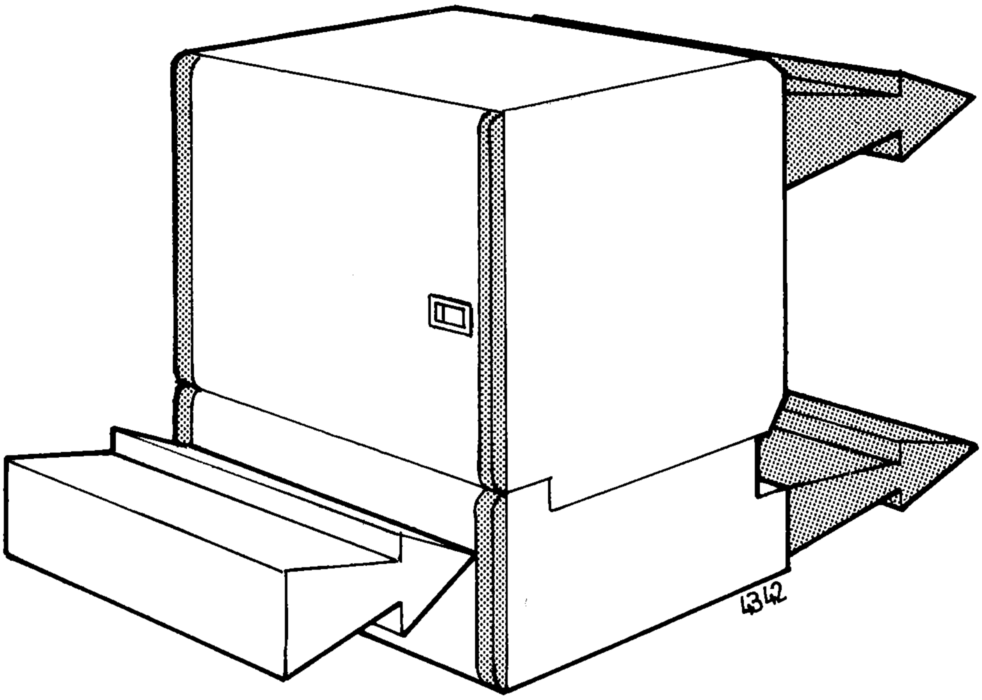


Figure 2.2.1 Harry Crate Assembly Air Flow.

(b) PTD M2350A DISC DRIVE AIR FLOW

The Disc drive units cool front to back as shown below.

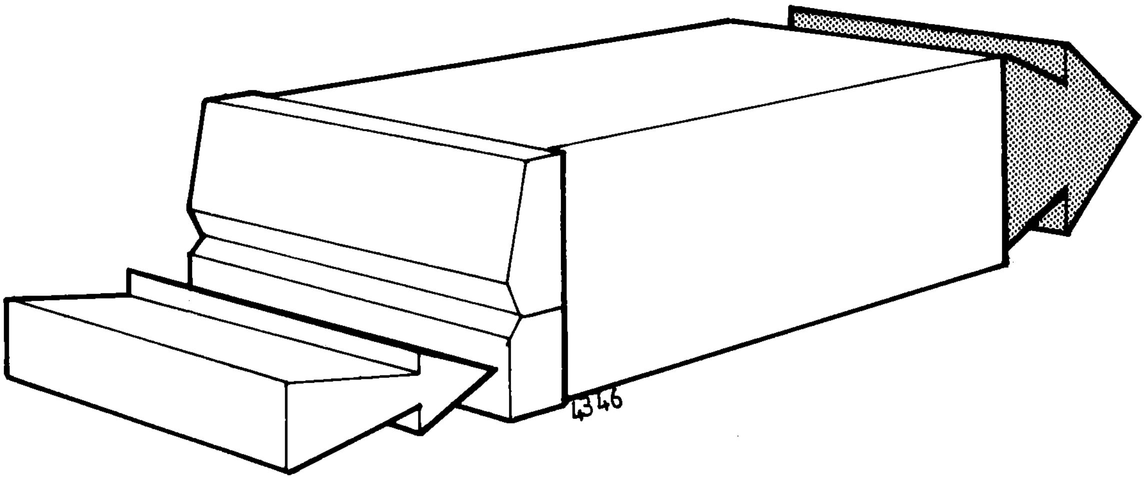


Figure 2.2.2 PTD Disc Drive Air Flow.

(c) PAINTBOX AIR FLOW

The Paintbox crate assembly cools front and right to back; that is cool air is drawn through the front panel and the right hand panel, and blown out at the left hand panel. Ensure that there is adequate clearance between the side panels and the cabinet to allow the Paintbox to be correctly cooled. The Paintbox front panel should be left closed during operation to allow even distribution of air within the card frame.

(d) PAINTBOX DISC DRIVE AIR FLOW

The Paintbox system can be operated using a number of different DISC Drive types. See the Disc Drive manuals for details of air flow.

SECTION 3 : UNPACKING

2:3:1 General

This section covers the unpacking and handling of equipment as it was delivered. Use the shipping list and the content guide to check that all contents are correct and that no damage has occurred in transit.

Care should be taken when unpacking the equipment, to ensure that all packing material is removed, from around the individual units and their connectors.

Figures 2.3.1 to 2.3.4 give details of the individual units for identification purposes.

WARNING: Read the Unpacking and Handling instructions before attempting to lift any part of the Harry system as each unit weighs approximately 95 kilograms.

FIGURES 2.3.1 & 2.3.2 HARRY UNIT AND PSU

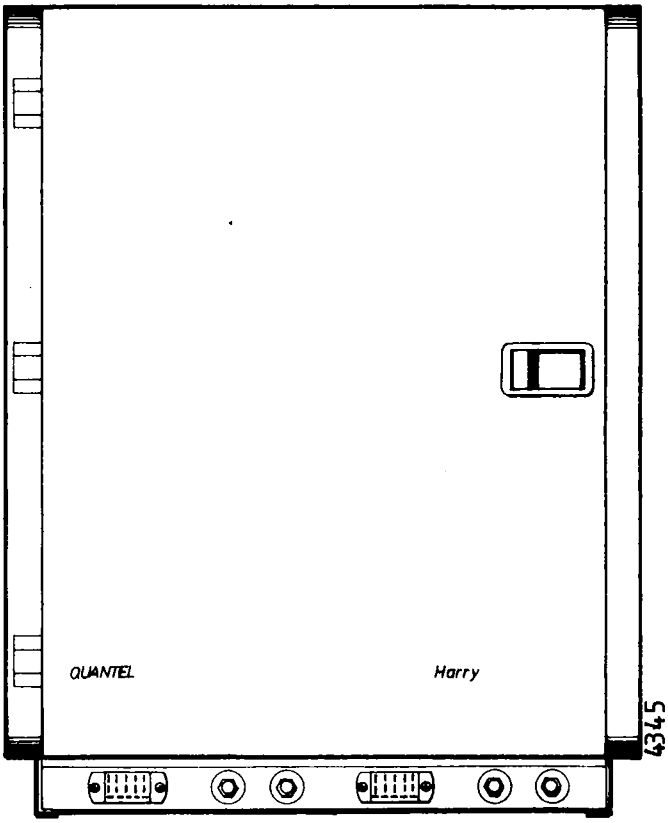


Figure 2.3.1 The Harry Unit.

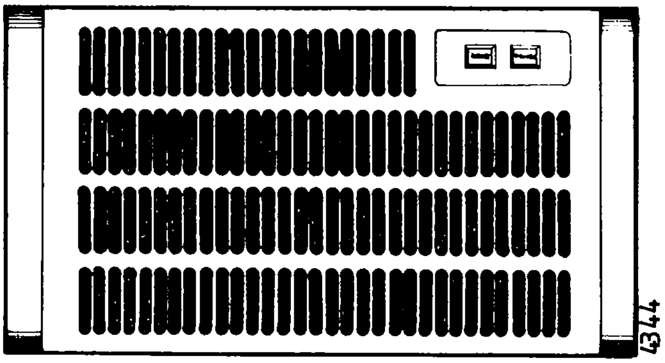


Figure 2.3.2 The Power Supply Unit.

FIGURES 2.3.3 AND 2.3.4 DISC DRIVE UNIT AND TABLET

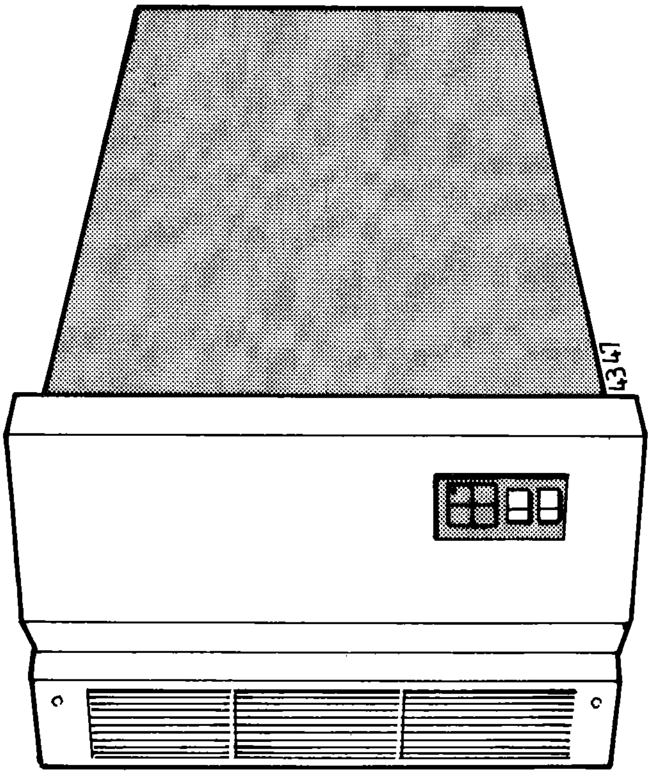


Figure 2.3.3 The PTD M2350A Disc Drive Units.

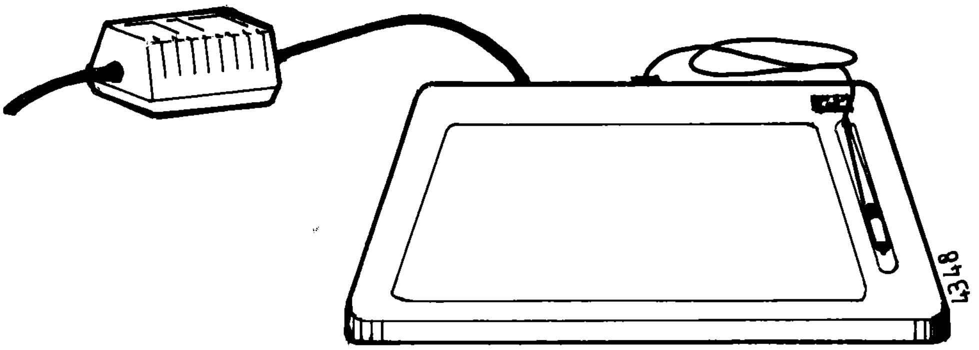


Figure 2.3.4 The TDS Digitized Tablet and Pen. This is supplied when a Paintbox is not to be used with the Harry system.

2:3:2 Handling The Harry Crate Assembly

It is recommended that five people should be used to remove the Harry crate assembly from its packing and to mount the crate in the cabinet to avoid damage to the unit and those who are unpacking it.

There are two "bolt on" handles provided on the Harry Crate assembly; one either side of the crate assembly. These are fitted before shipment and are removed when unit is being fitted into the cabinet.

It is suggested that one person holds the packing still while two people, either side of the crate, lift the crate assembly straight up and out of the packing. The packing can then be removed from beneath.

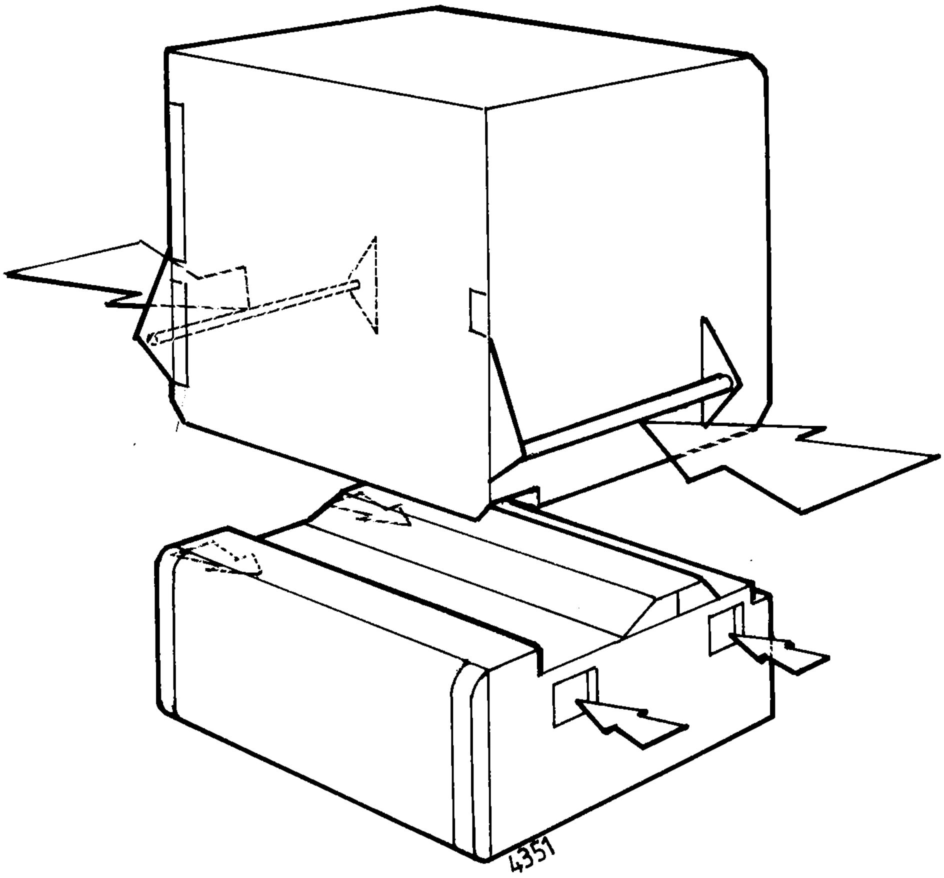


Figure 2.3.5 Harry Crate assembly Handles

2:3:3 Handling The Disc Drive Units

The four Disc Drive units are marked as Top Left (TL), Top Right (TR), Bottom Left (BL) and Bottom Right (BR). Each Disc Drive unit has a designated place within the cabinet and therefore should be unpacked as they are required.

It is recommended that five people or a Fork-Lift should be used to remove the Disc Drive units from their packing to avoid damage to the units and those who are unpacking them.

There are four fabric handles provided on the Disc Drive units, which are fitted to the underneath of the unit. It is recommended that four people, two either side, lift the Disc Drive unit straight up from the packing, while the fifth person removes the packing from beneath the Disc. The Disc should be placed on a pallet or two pieces of wood so that the fabric handles can be removed and the rack slides can be fitted.

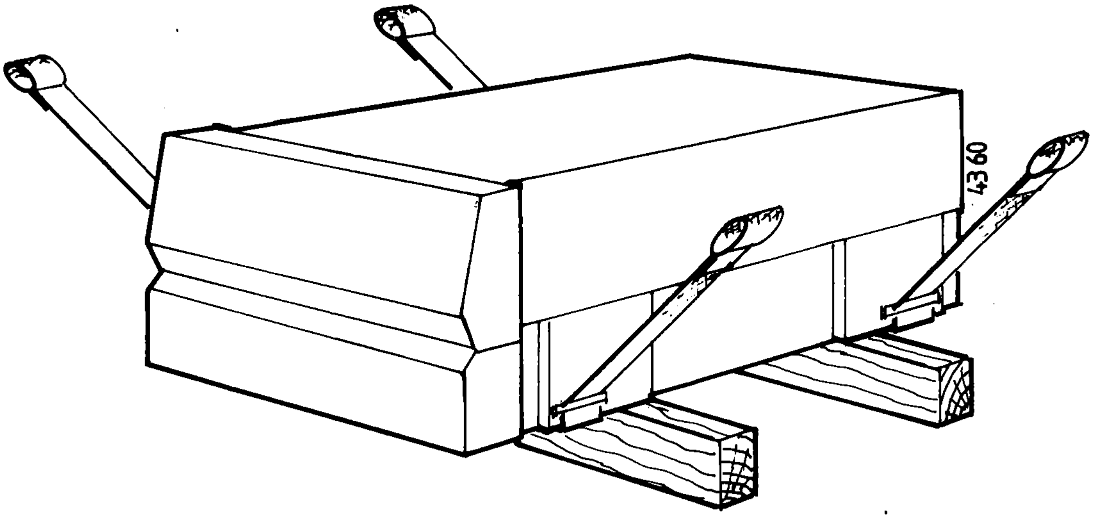


Figure 2.3.6 Disc Drive Unit Handles

(2,3A)

FIGURE 2.3.7 HARRY CRATE ASSEMBLY PACKING DIAGRAM

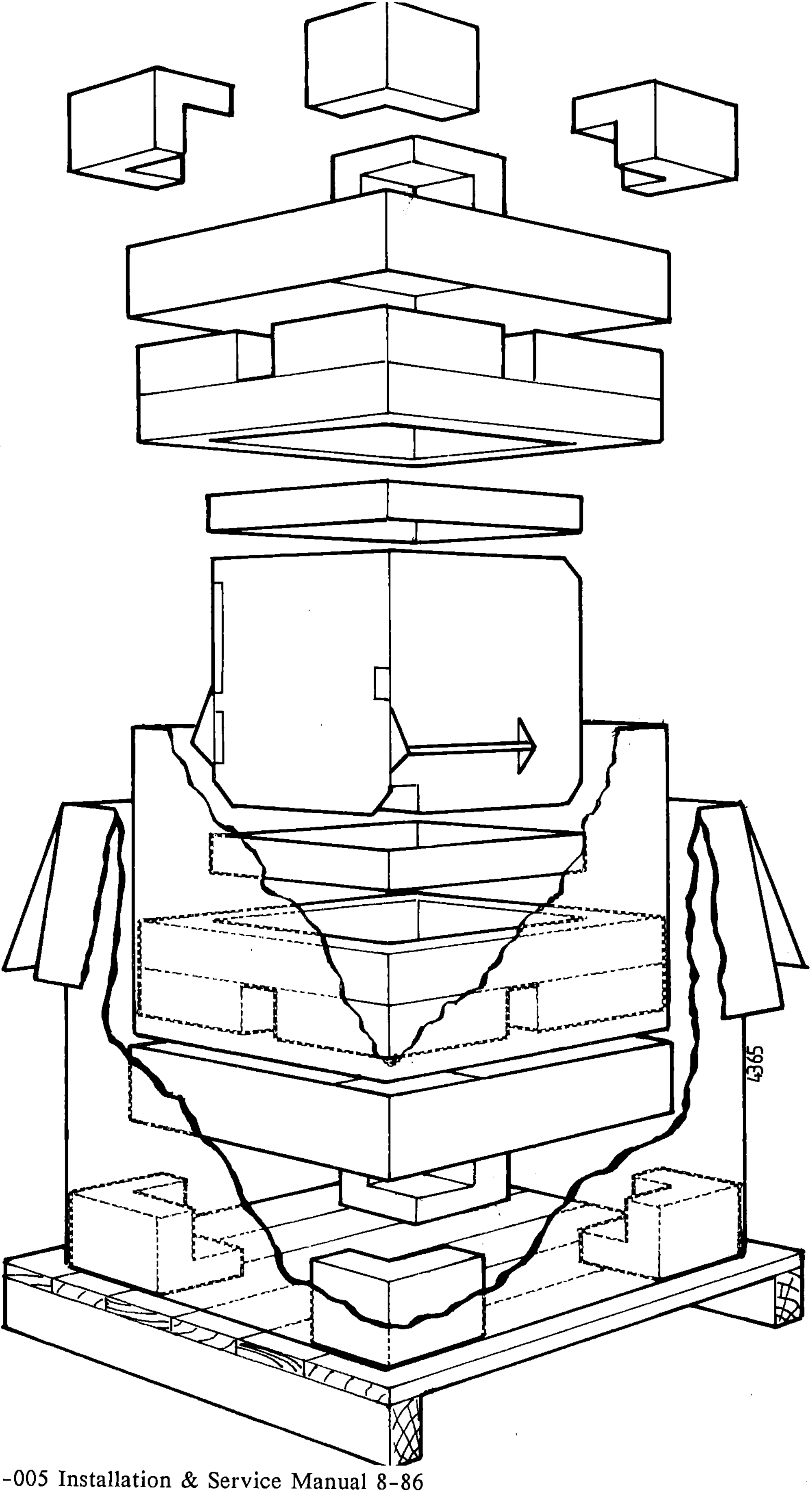


FIGURE 2.3.8 POWER SUPPLY UNIT PACKING DIAGRAM

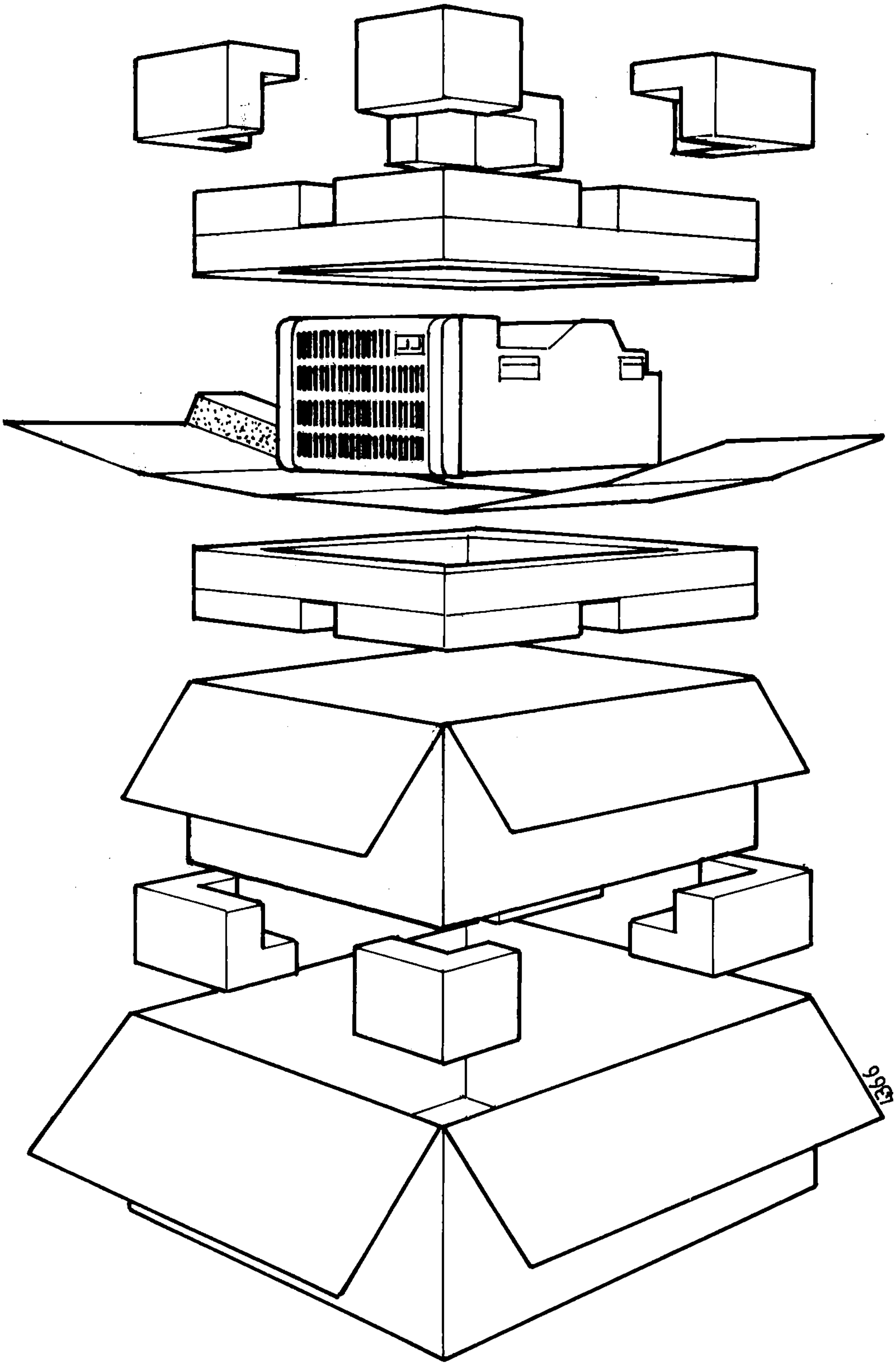


FIGURE 2.3.9 DISC DRIVE UNIT PACKING DIAGRAM

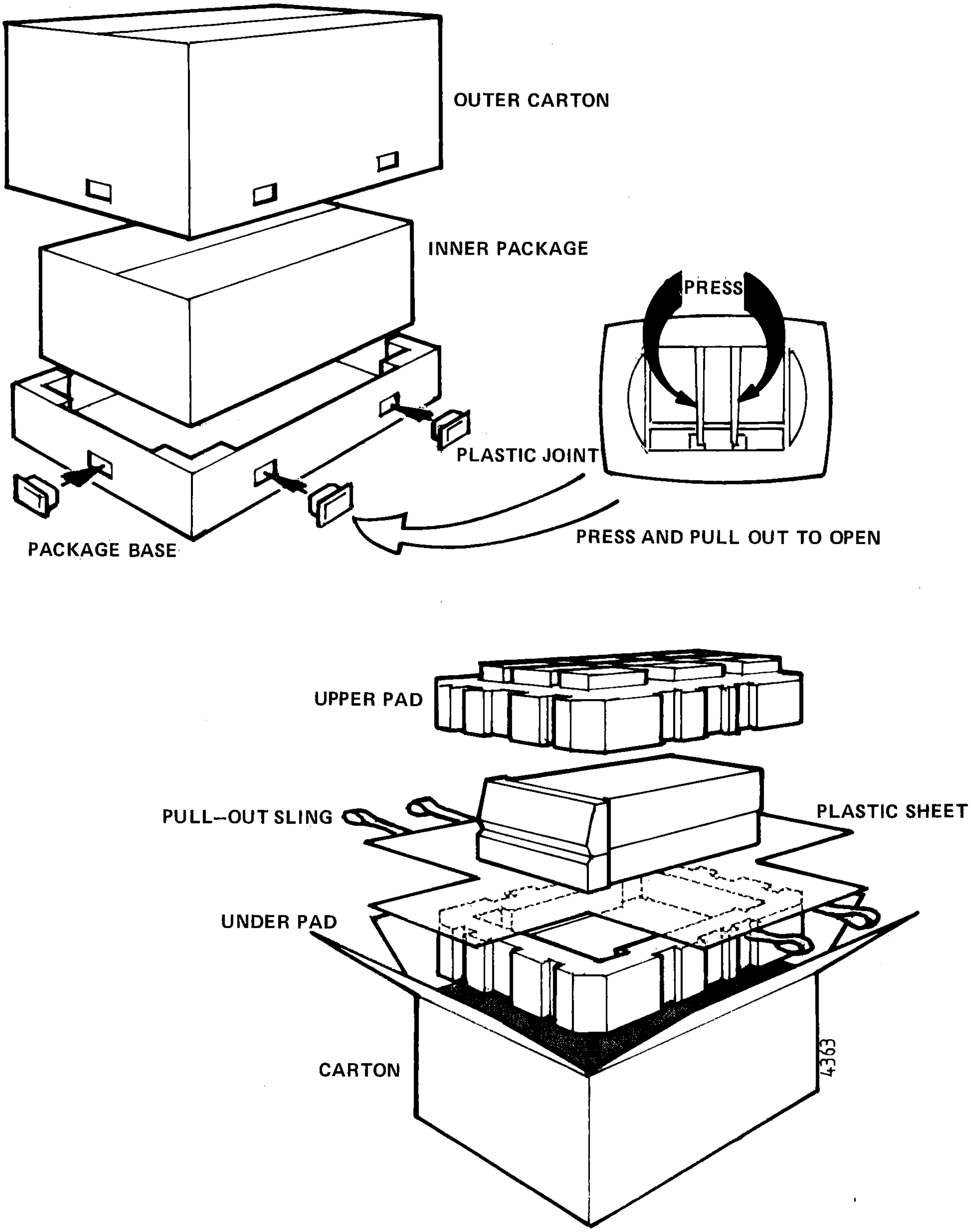
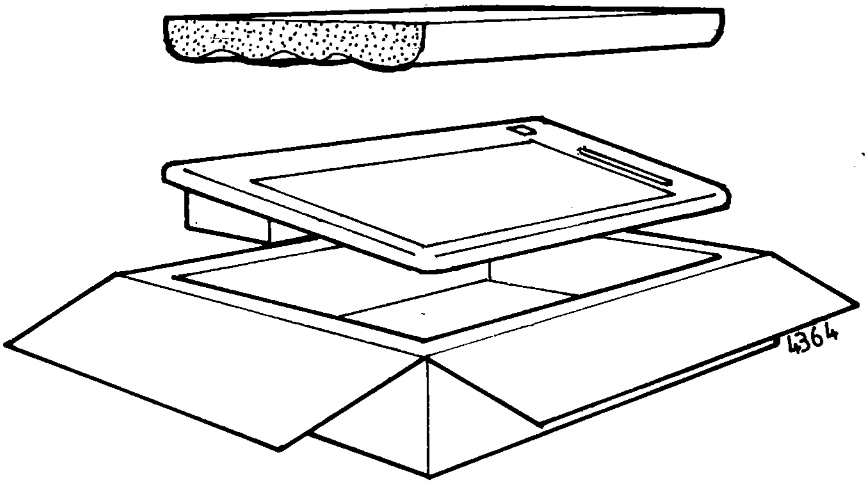


FIGURE 2.3.10 TDS TABLET PACKING DIAGRAM



SECTION 4 : RACK MOUNTING

2:4:1 General

The cabinets required to house the Harry system are 19" (483mm) wide (inside) with a depth of 27" (685mm). The Harry system requires two 6 foot high cabinets. The system is supplied with a rack mounting kit which includes rack slides and re-enforcing plates which should be fitted as described in the following pages.

The two cabinets which are to hold the complete Harry system should be side by side and the system should be located as shown in Figures 2.4.1 to 2.4.3. The right hand cabinet holding the 4 Disc drive units and the left hand cabinet holding the Harry crate assembly, Power supply unit, the Paintbox system and its Disc drive unit.

The Harry system units should be fitted into the cabinets as shown in figures 2.4.1 to 2.4.3. The cabinets should be fitted with units bottom to top to prevent the cabinets falling forward.

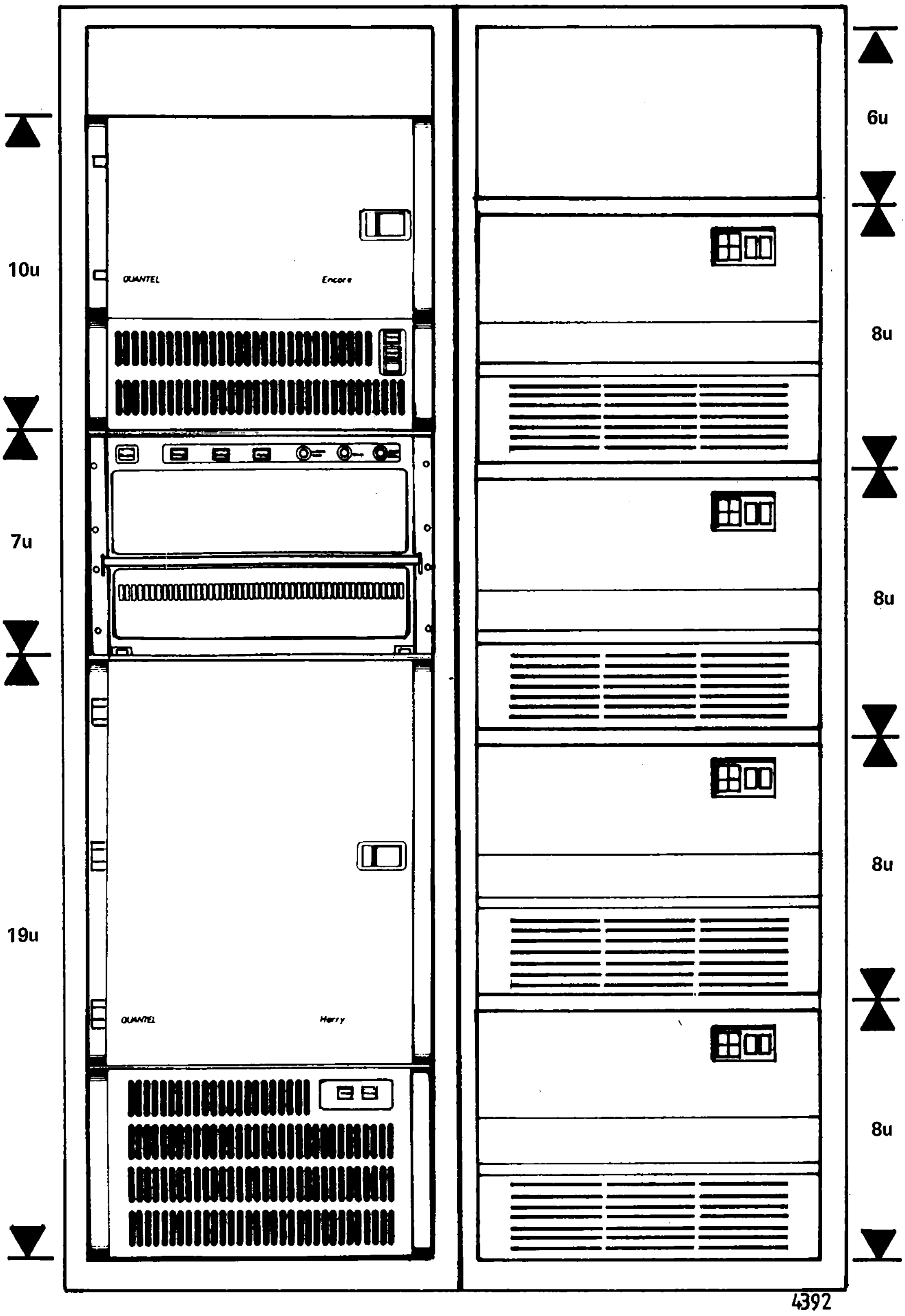
WARNING: NEVER HAVE MORE THAN ONE UNIT ON EXTENDED RACK SLIDES AS THIS MAY CAUSE THE CABINET TO FALL OVER.

2:4:2 Harry Crate Mounting Procedure

The following procedure gives detailed instructions on how to rack mount the Harry system. Please read the following instructions carefully before rack mounting the system. See figures 2.4.1 to 2.4.7

(2,4A)

FIGURE 2.4.1 HARRY/PAINTBOX/ENCORE 4-DISC CONFIGURATION



(a) MOUNTING RE-ENFORCING PLATES

Locate and mount the four re-enforcing bars (40/01/3294U) as shown below.

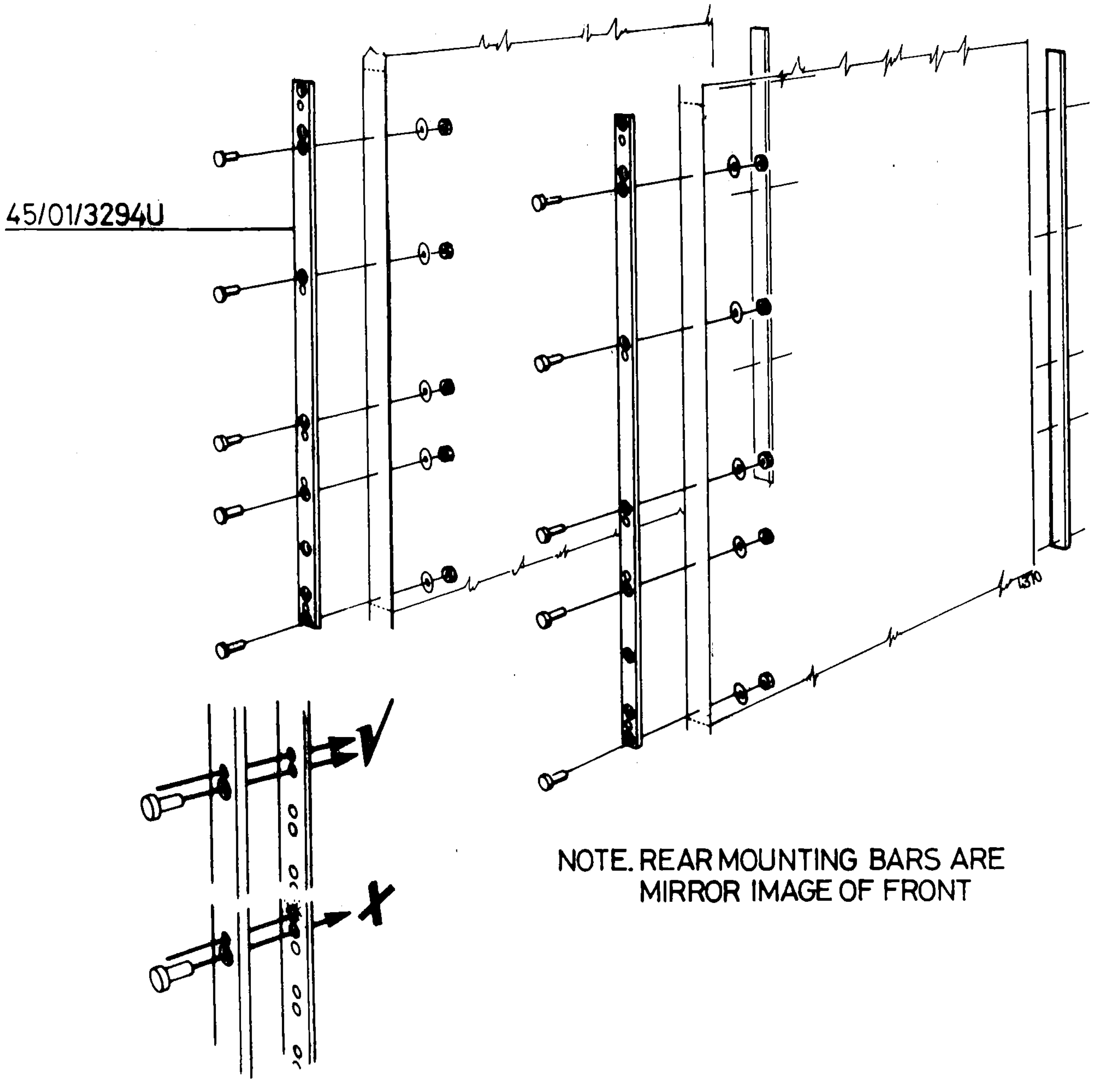
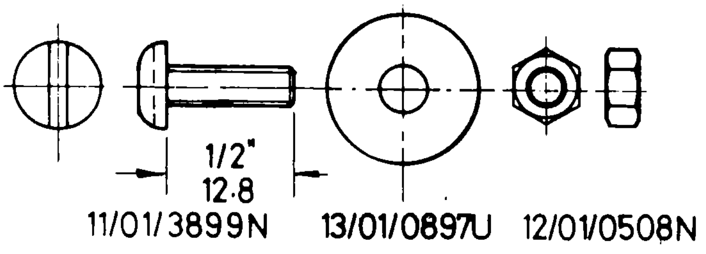


Figure 2.4.2 Mounting Re-enforcing Plates



(b) MOUNTING SLIDES INTO THE CABINET

Locate and mount the four slides (55/02/0159N) with the eight mounting bars (45/01/2565U) and the side supports (43/01/2657U) as shown below.

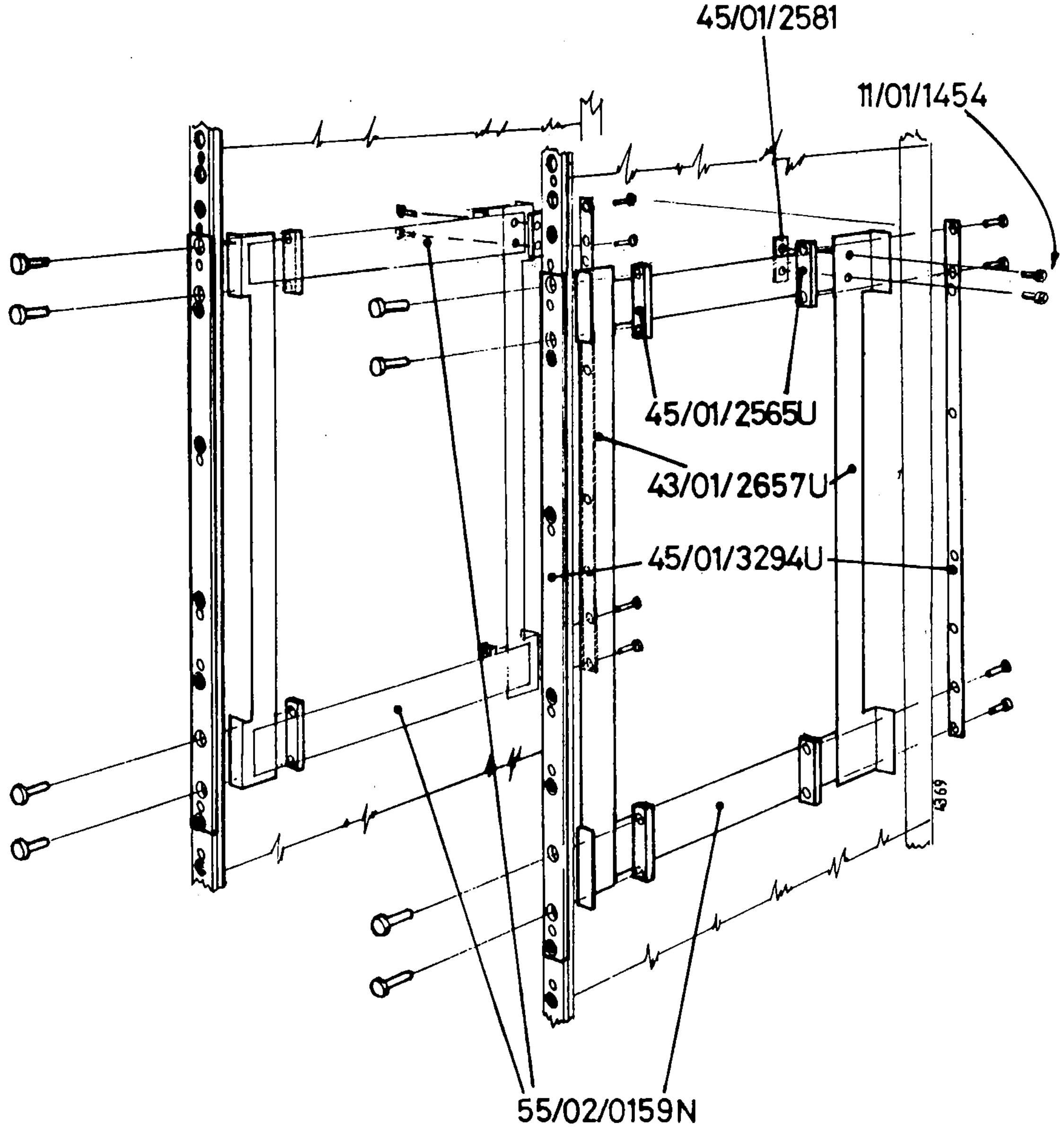
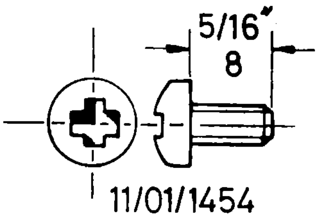
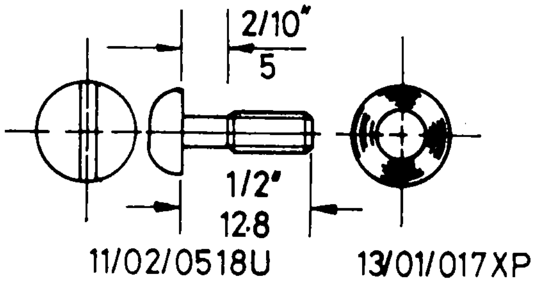


Figure 2.4.3 Mounting the Slides into the Cabinet.





(c) MOUNTING THE CRATE INTO THE CABINET

Caution: Five people are required to guide the crate assembly into the slides; four people to lift the crate, and one person to guide and stop the cabinet moving.

i. Fit the crate assembly into the rack mounted slides, ensuring that the catches are on before sliding the crate assembly into the rack. With the crate inserted part way into the rack, remove the crate's handles.

ii. Slide the crate fully into the rack and fit the mounting bolts to secure the crate assembly into the rack as shown below.

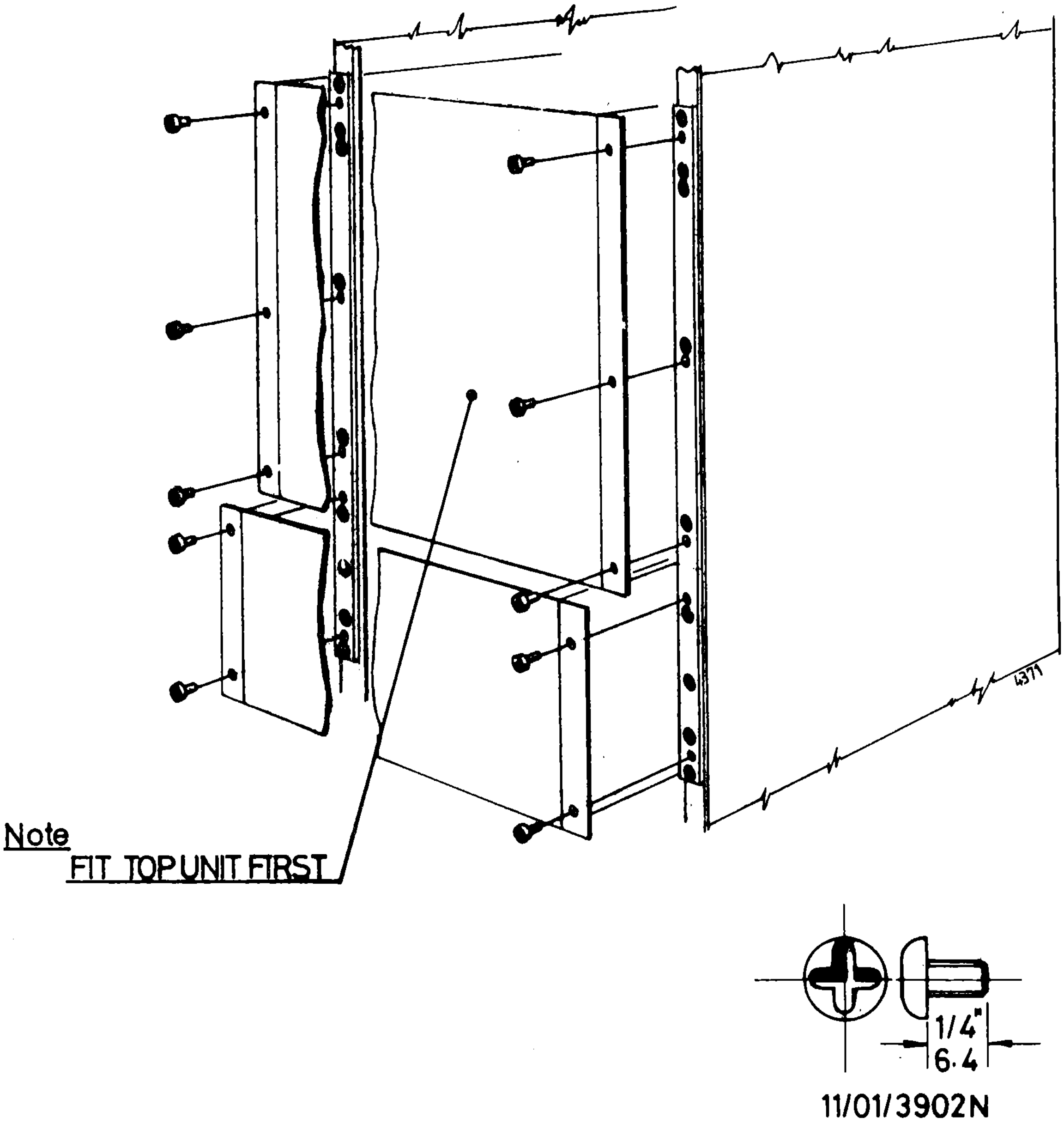


Figure 2.4.4 Mounting the Crate into the Cabinet.

(d) REMOVING THE RETAINING PLATE

i. The Harry crate assembly is transported with a PCB retaining plate fitted, to reduce movement in the card frame while in transit. The retaining plate is mounted across the front of the card frame and the PSU housing. The retaining plate should only be removed after the Harry crate assembly has been installed in its rack.

ii. Remove the screws at the top and bottom of the retaining plate and remove the plate from the crate assembly. Remove the wooden packing block from the bottom of the crate assembly.

iii. Store the retaining plate for future transport of the crate assembly.

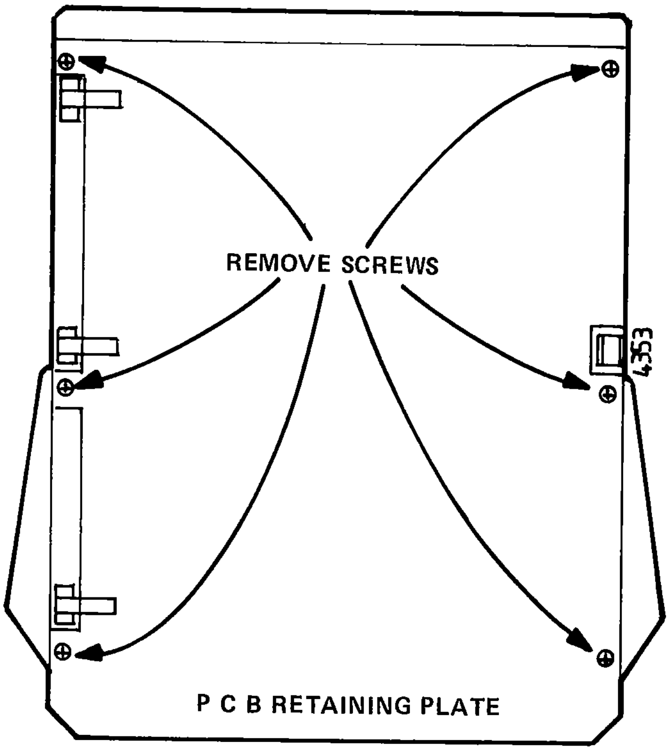


Figure 2.4.5 Removing the Retaining Plate.

2:4:3 Harry PSU Rack Mounting Procedure

(a) When the crate assembly has been rack mounted and the PCB retaining plate has been removed, the power supply unit should be fitted as soon as possible to avoid foreign matter entering the PSU housing and the power connectors. Fitting the PSU is a simple process and therefore the following may be regarded as guide lines:

(b) Before inserting the PSU, check that the PSU connectors have not been damaged in transit and that they are free from any packing material.

(c) Two people are recommended to slide the PSU into its slides in the cabinet.

(d) When the PSU is in place secure using the screws provided.

(e) When the Power supply unit has been fitted into the cabinet and the Harry crate, refit the crate assembly Front door.

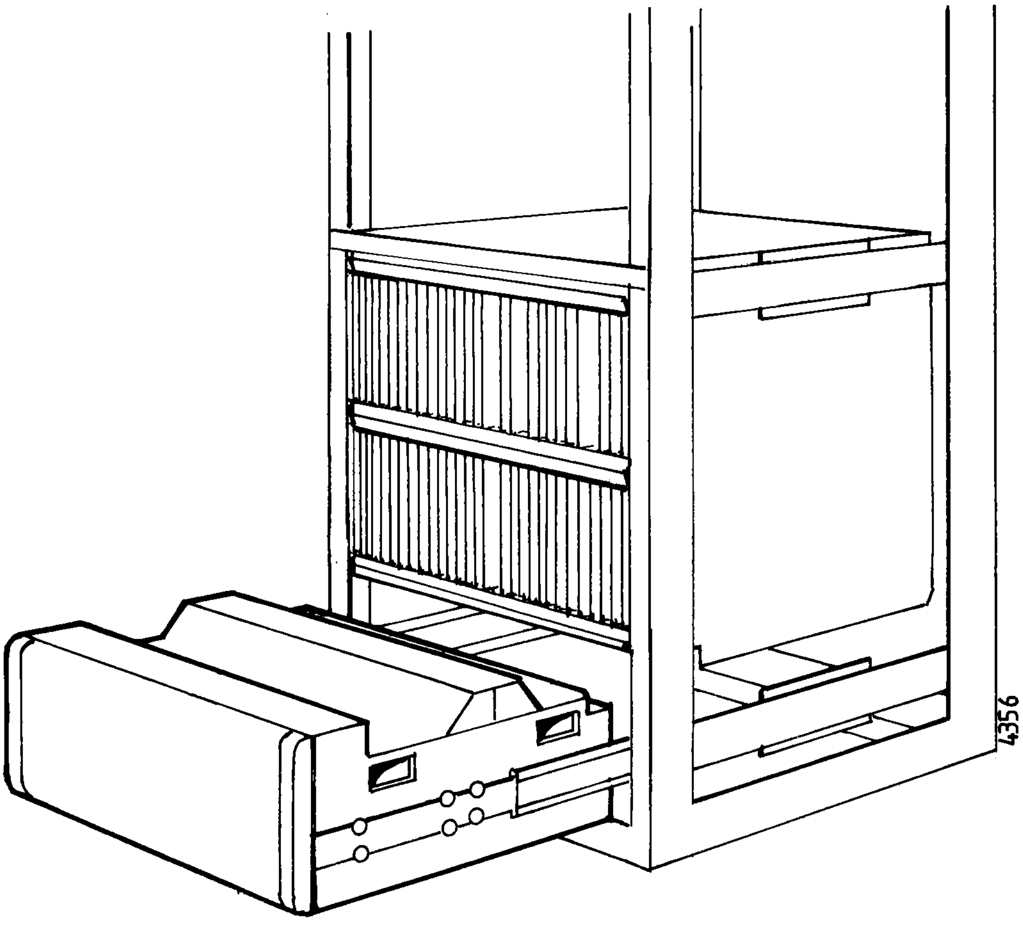


Figure 2.4.6 Rack Mounting The PSU Assembly.

(2,4A)

(f) Fit the front door and escutcheons to the crate as shown below.

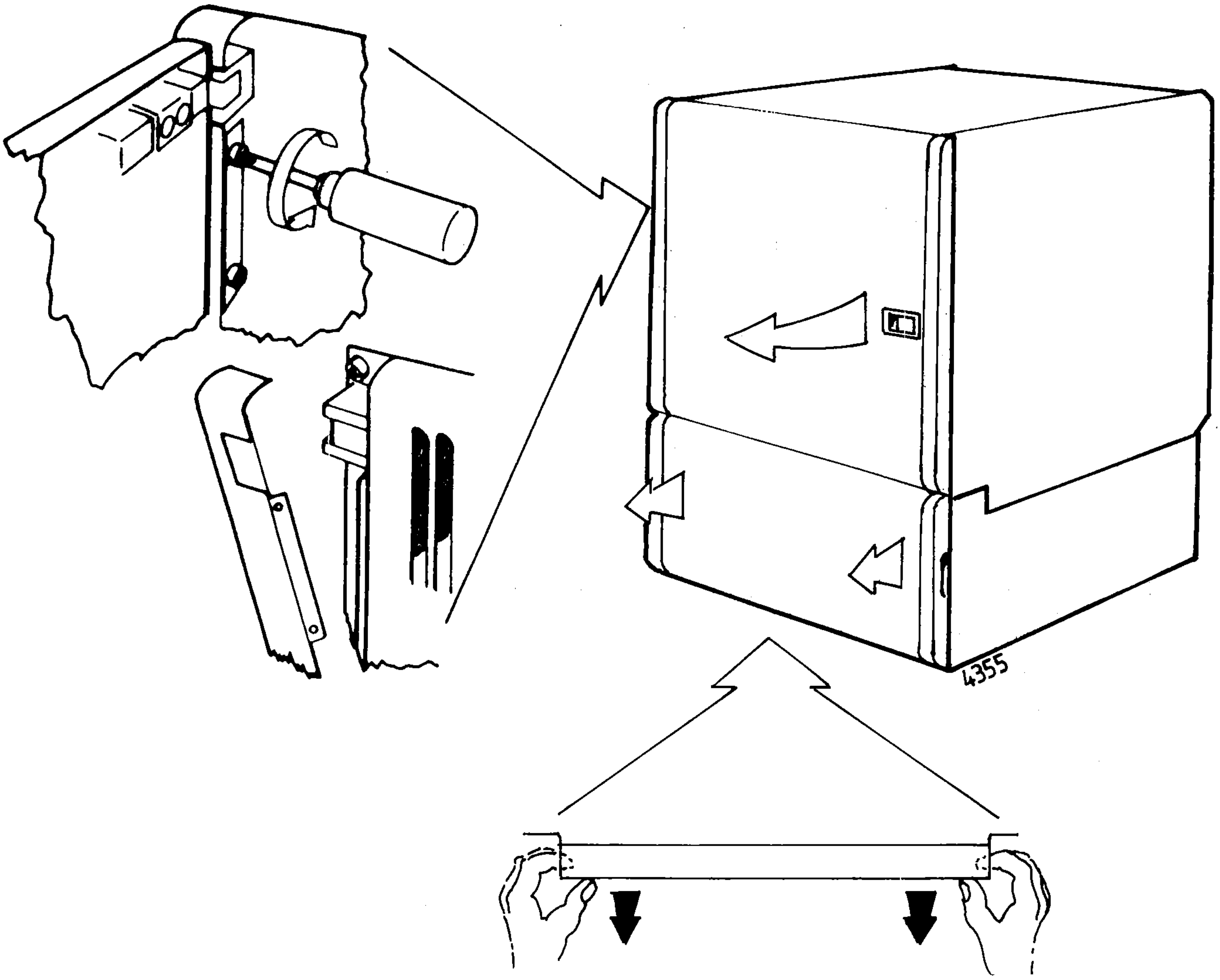


Figure 2.4.7 Fitting the Crate Front Door.

(2,4A)

2:4:4 Mounting the Disc Drives

Caution: Five people are required to guide the Disc units into the slides; four people to lift the Disc, and one person to guide the inner slide and to stop the cabinet moving.

(a) Before rack mounting the Disc Drive units remove the Disc transit locks as shown in the Disc Drive manual.

(b) Remove the fabric handles and the clamps from each Disc Drive unit and fit the inner slides to each side.

(c) Locate and fit all the outer Disc slides to the right cabinet and mount the Disc Drives into the cabinet as shown in figures 2.4.1.

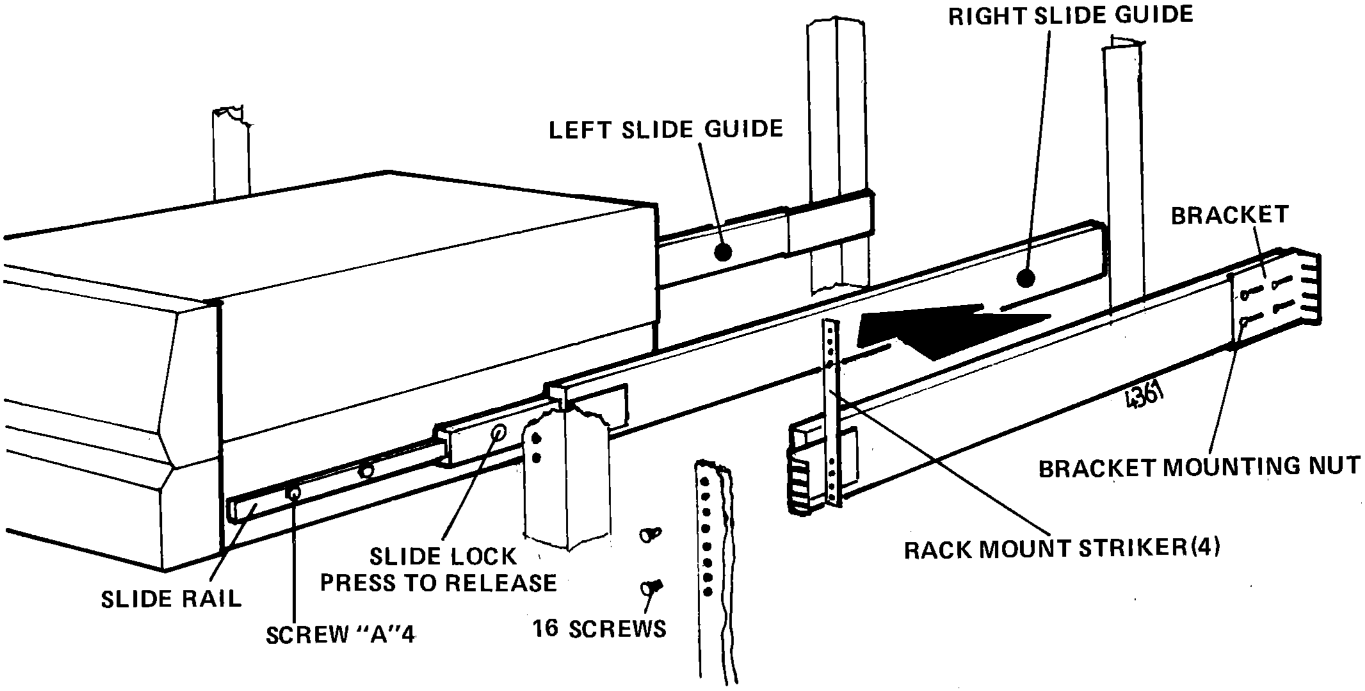


Figure 2.4.8 Rack Mounting the Disc Drive Units.

2:4:5 Cable Clamps and Screening

(a) GENERAL

When the Harry unit has been connected as described in section 5, the Disc cable clamps and the RFI screens should be fitted as described in this section.

(b) HARRY UNIT DISC CABLE CLAMPS

The Bus and Radial cables from the Harry unit should be secured to the rear panel of the Harry unit using the Cable clamp provided. This cable clamp is provided to prevent the Disc cable from falling out of their sockets under the weight of the cables. See figure 2.4.9 for details.

(c) PTD DISC DRIVE CABLE CLAMP

The Bus and Radial cables should be secured to the Disc Drives as shown in figure 2.4.9.

(d) CABLE SCREENS

Connect the Disc cable screens to the Disc Drive and Harry chassis and shown in figure 2.4.9.

FIGURE 2.4.9 CABLE CLAMPS AND SCREENS

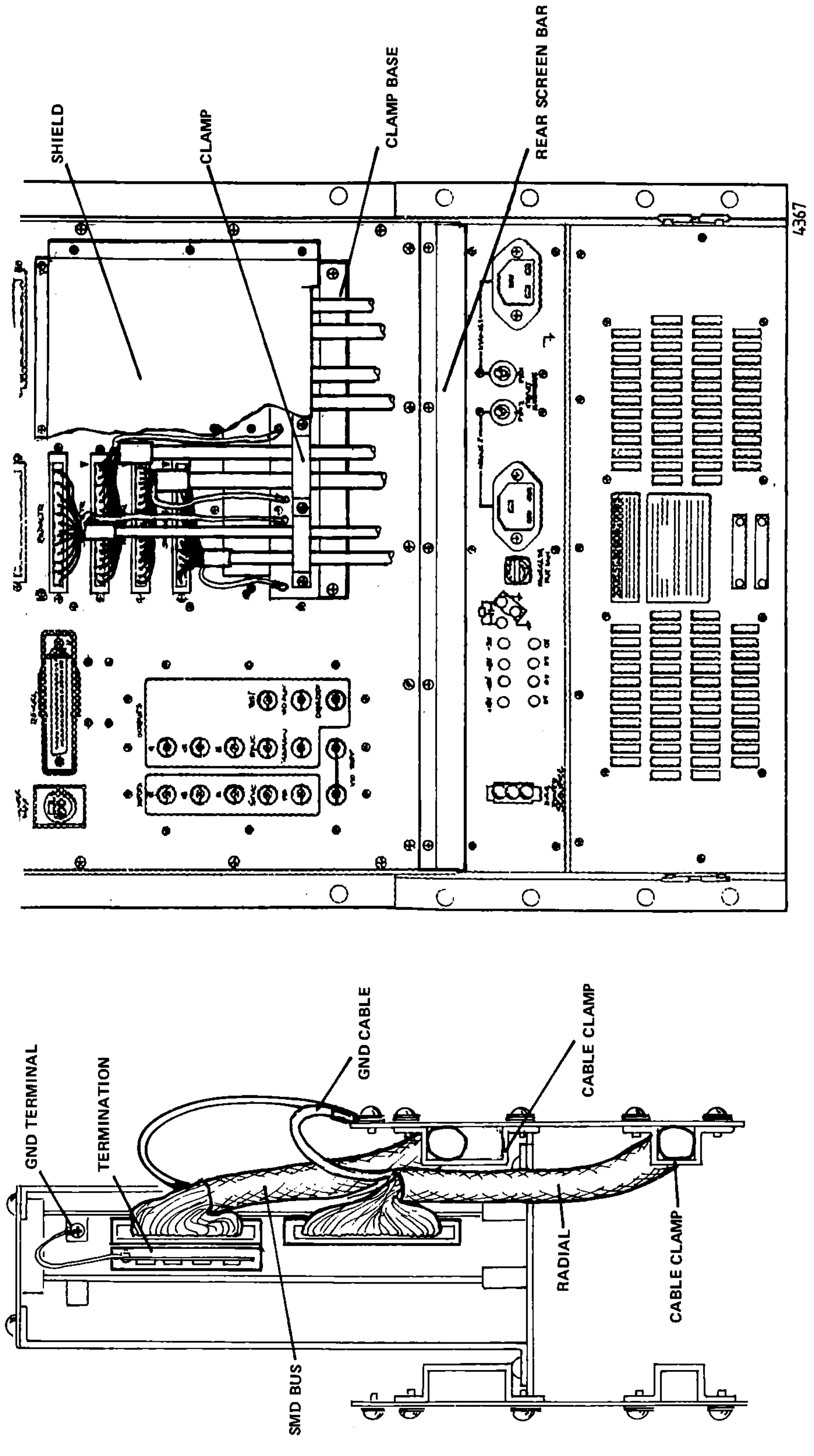


FIGURE 2.4.10 SYSTEM SOCKET LOCATION

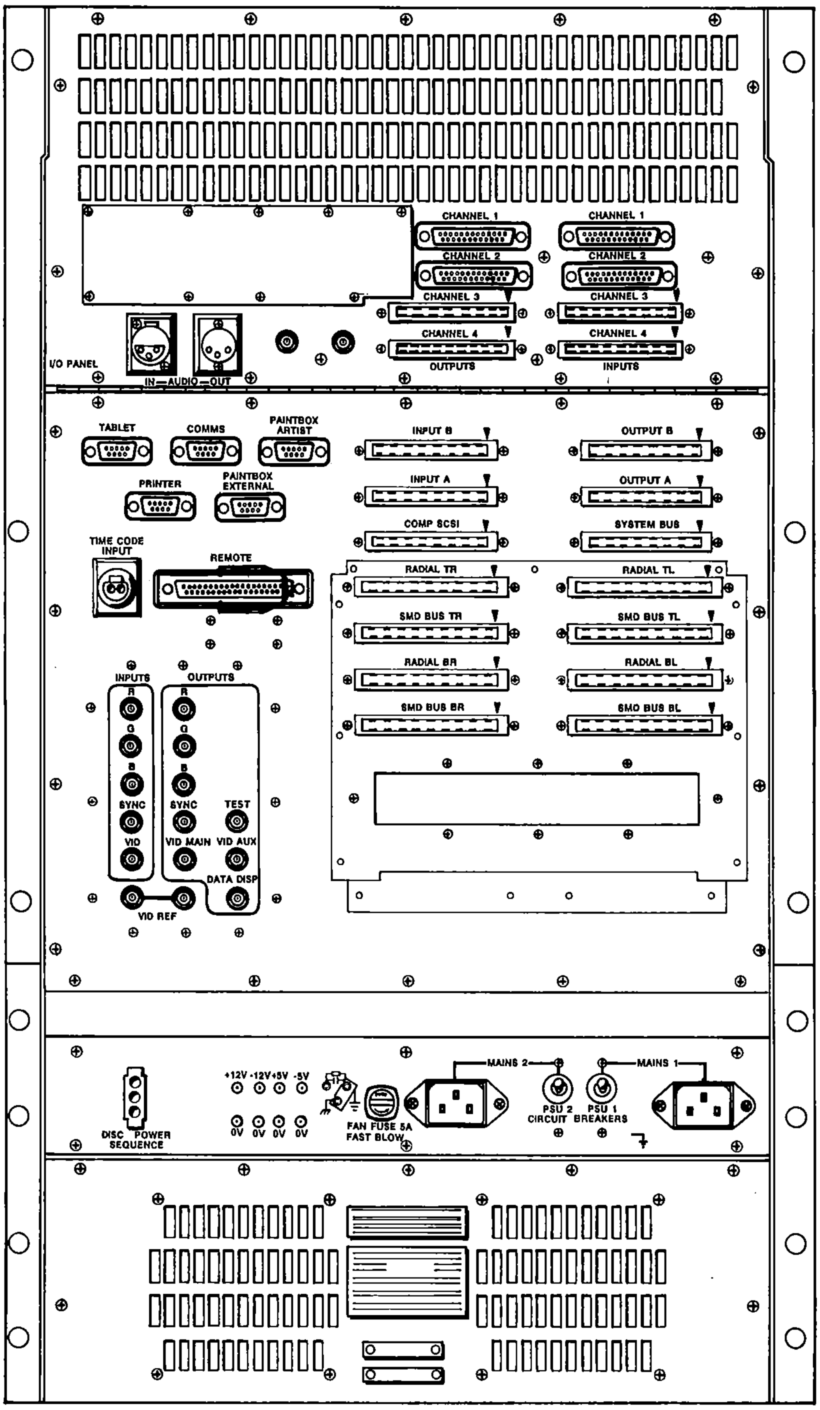
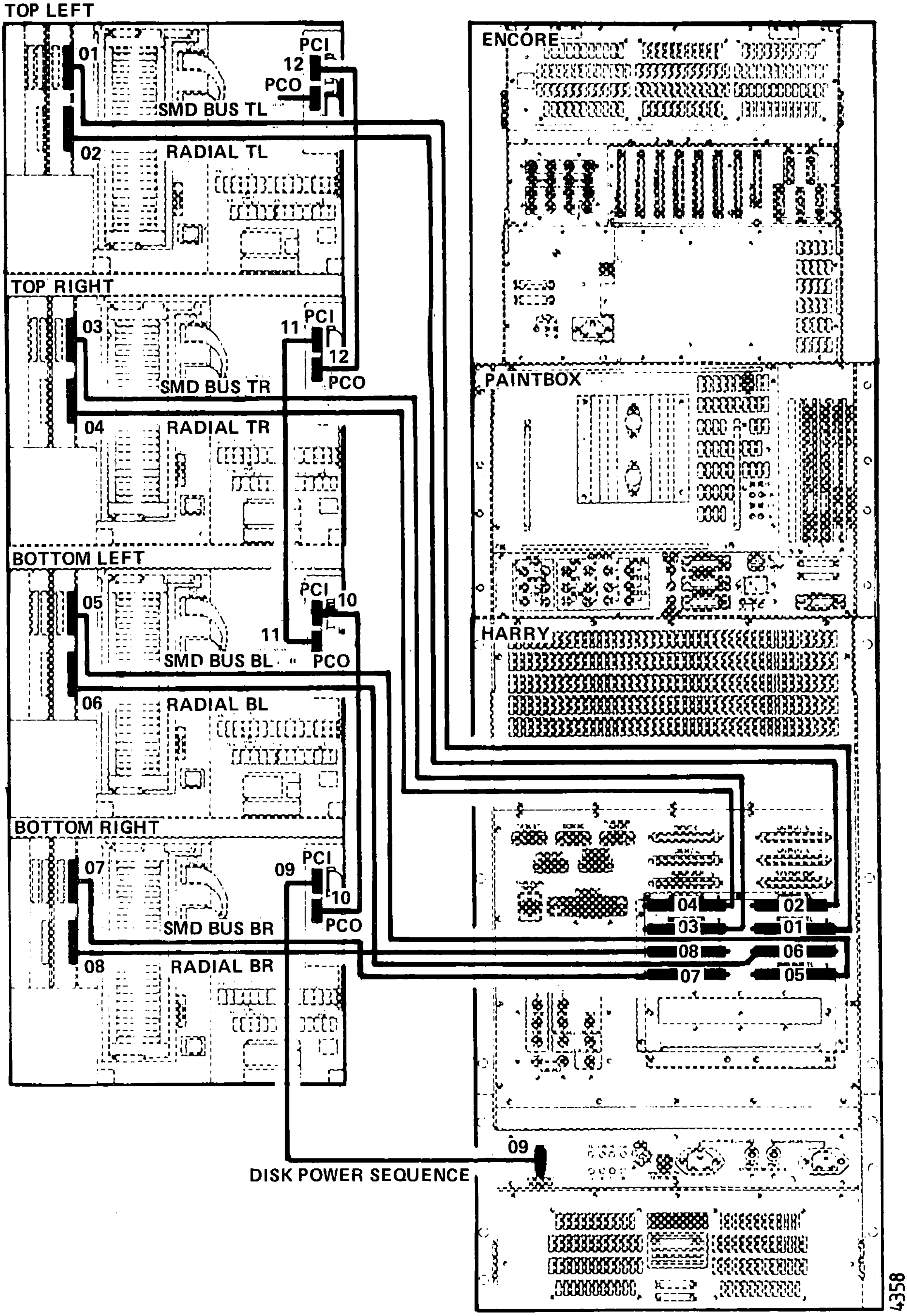


FIGURE 2.5.3 DISC DRIVE CONNECTION DIAGRAM



2:5:2 Data and Control Connections

Connect the Harry unit to the Paintbox and Encore unit as shown in figures 2.5.2 and 2.5.3. Connect the Disc Drive units to the Harry unit as shown in figure 2.5.3.

(a) DISK CONNECTIONS (Figure 2.5.3)

NO.	HARRY	CABLE	DISC
01	SMD BUS TL	EA0-10900A010A8	SMD BUS TL
02	RADIAL TL	EA0-10900A010A8	RADIAL TL
03	SMD BUS TR	EA0-10900A010A8	SMD BUS TR
04	RADIAL TR	EA0-10900A010A8	RADIAL TR
05	SMD BUS BL	EA0-10900A010A8	SMD BUS BL
06	RADIAL BL	EA0-10900A010A8	RADIAL BL
07	SMD BUS BR	EA0-10900A010A8	SMD BUS BR
08	RADIAL BR	EA0-10900A010A8	RADIAL BR
09	POWER SEQ	B2000-T507A	BR PCI

NO.	DISC	CABLE	DISC
10	BR PCO	B2000-T507A	BL PCI
11	BL PCO	B2000-T507A	TR PCI
12	TR PCO	B2000-T507A	TL PCI

(b) PAINTBOX CONNECTIONS (Figure 2.5.2)

NO.	HARRY	CABLE	PAINTBOX
13	INPUT A	EAO-10900A006BX	SKT 1
14	OUTPUT A	EAO-10900A006BX	SKT 2
15	PAINTBOX	EAO-10900A008A6	ARTIST
16	TEST	EAO-10900A014AY	PRINTER

(c) ENCORE CONNECTIONS (Figure 2.5.2)

NO.	HARRY	CABLE	ENCORE
17	INPUT B CHANNEL 4	EAO-10900A006BX	DIGITAL VID OUT
18	OUTPUT B CHANNEL 4	EAO-10900A006BX	DIGITAL VIDEO IN
19	REMOTE	EA- 2003511-701	EXTERNAL TAKE

SECTION 5 : EXTERNAL CABLE CONNECTIONS

2:5:1 Video Signal Connections

(a) HARRY

The input and output video connections should always be made to the Harry crate. Connect up the Harry system video signals as shown in figure 2.5.1 and see chapter 1 for input and output video specifications. The input video and reference signals should always be connected to the Harry unit.

(b) PAINTBOX

When Paintbox is connected to the Harry system (via Input a and Output A) the Paintboxes input timing references are provided by the Harry unit, but, ~~Paintbox~~ the output timing references are provided by the Paintbox.

The Paintbox should be connected for normal operation, with the Paintbox using the same output reference video as the Harry unit. The Paintbox's video inputs and outputs are available for use when Harry is not buying or selling pictures. The input video and reference signals should always be connected to the Paintbox unit.

(c) ENCORE

When Encore is connected to the Harry system (via Channel 3 or 4) the Encore's input timing references are provided by the Harry unit, but, the Encore's output timing references are provided by the Encore unit.

The Encore should be connected for normal operation, with the Encore using the same output reference video as the Harry unit. The Encore's video inputs and outputs are available for use when Harry is not accessing the Encore. The input video and reference signals should always be connected to the Encore unit.

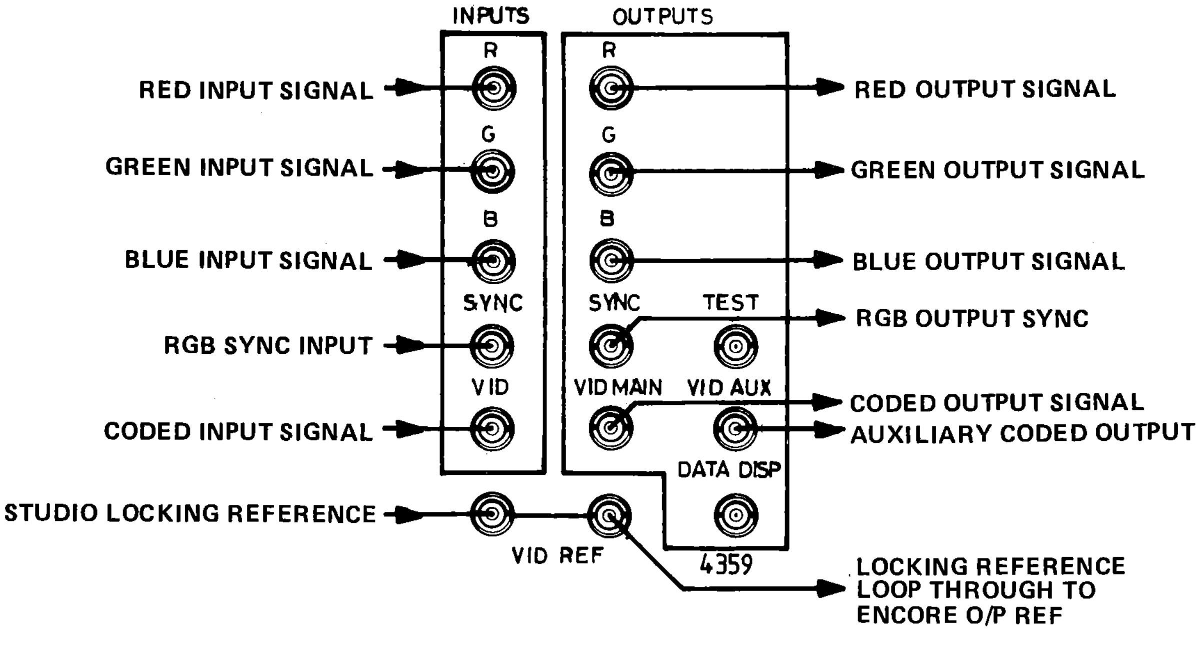
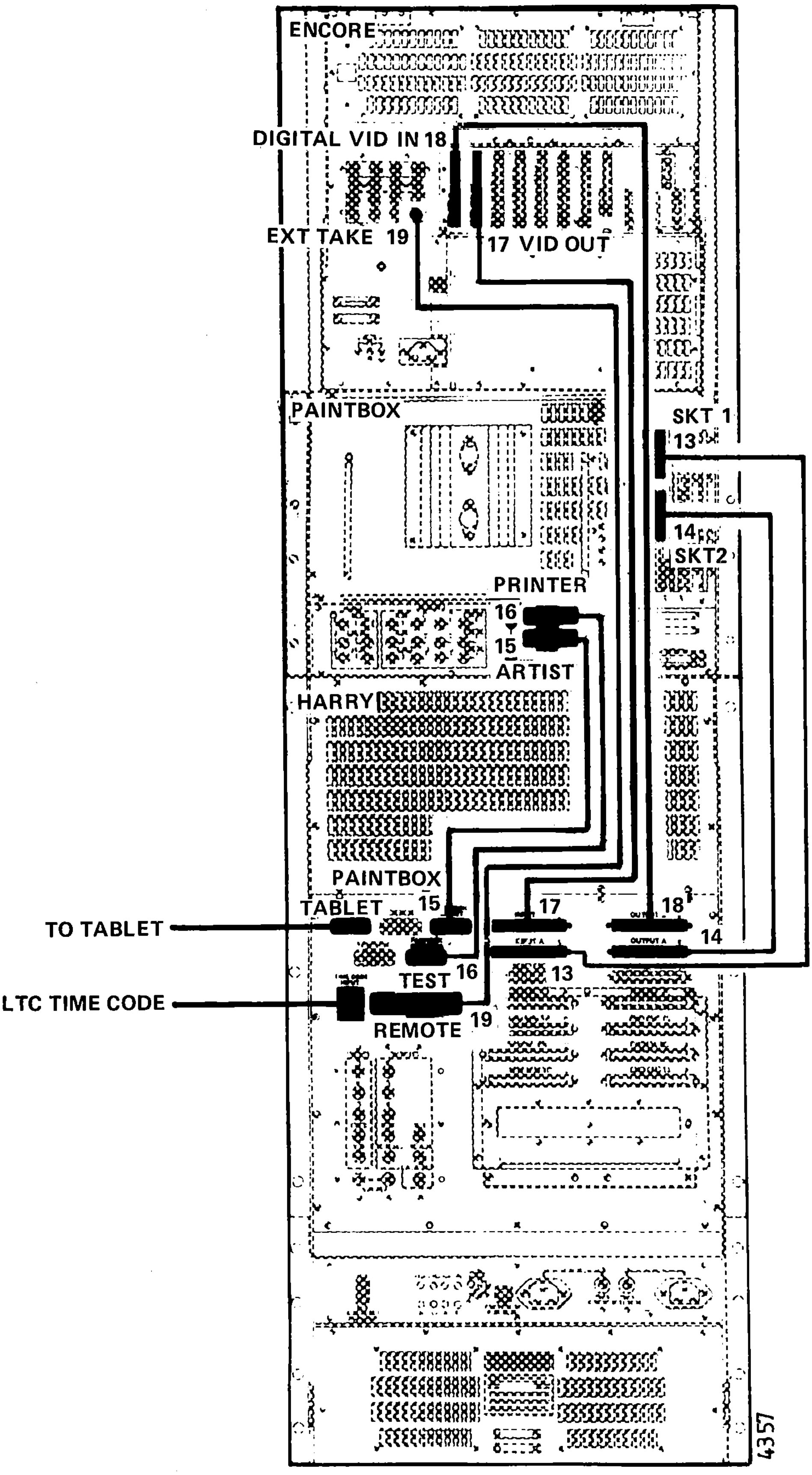


Figure 2.5.1 Video Signal Connections

FIGURE 2.5.2 HARRY/PAINTBOX/ENCORE CONNECTIONS



2:5:3 External Cue Connections

(a) GENERAL

The Harry system provides 4 Cue inputs accessed via the "Remote" connector on the Harry crate rear panel. The remote cue lines are examined by the system computer shortly (0 - 4 mS) after each field interval. Hence to ensure that a cue input is recognised, the remote cue should be present for at least one whole field.

(b) INPUT CUES

There are 4 input Cues, which can be used to trigger Record and Replay operations within the Harry system. The system can be triggered by connecting or disconnecting 0 volts on the appropriate input cue line of the Remote socket on the rear panel of the Harry unit. The cue lines are connected as follows:

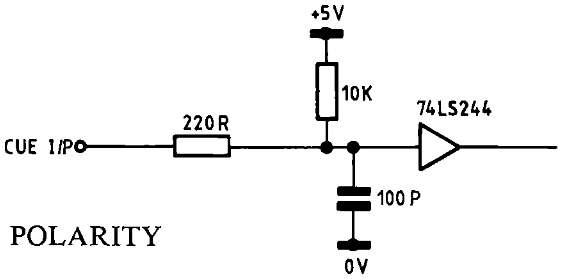
Input Cue 1	pin 17 of the Remote socket.
Input Cue 2	pin 16 of the Remote socket.
Input Cue 3	pin 15 of the Remote socket.
Input Cue 4	pin 14 of the Remote socket.
0 volt (ground)	pins 29,33,34,35

Remote Cues

The input cue can also be triggered by TTL level signals:

Logic "0" = 0 to +2.4V Logic "1" = +2.4 to 5.5V

The input cue is received in Harry by the 74LS244 circuit shown:



(c) CUE POLARITY

A cue input can be of either polarity. Each time the "Go" box on the Record or Play menu is pressed, Harry will note the level of the cue and assume that this is the "No-cue" state.

(d) OUTPUT CUES

The Harry system provides 12 cue outputs. These are produced by 12 pairs of independent Relay contacts, which are closed when an output cue occurs. The relay characteristics are as follows:

Switch voltage (max)	100V DC
Switch current (max)	0.5 Amps
Switch power (max)	10W
Contact resistance	0.1 ohms

(2,5B)

A current limited +5 volt supply is provided so that logic level cues can be produced. Connect up the output cue lines as follows:

Output Cue	Remote Socket	Function
1	pins 8 & 27	
2	pins 7 & 26	
3	pins 6 & 25	
4	pins 5 & 24	
5	pins 4 & 23	
6	pins 3 & 22 -	[illegible] - used to slack 20 P/[illegible]
7	pins 2 & 21	Encore VDU
8	pins 1 & 20	Harry VDU [illegible] monitor [illegible]
9	pins 9 & 28	Ready to record
10	pins 11 & 30	Recording
11	pins 12 & 31	Ready to play
12	pins 13 & 32	Playing (Ext Cue Encore)

+5 volts (50mA) pins 18 and 19 of the Remote socket.

(e) RECORD CUE TIMING (Software version 1.17 onwards)

Cue 10 ("Recording") will close after the 3rd field boundary (without ST) or the 10th field boundary (with ST enabled) following a Cue input. The frame in which Cue 10 closes is the first frame to be recorded. Cue 10 will open in the first field (7-10 mS after the field boundary) of the frame after recording.

Note that for software versions prior to V1.17, Cue 10 closes after the 1st field boundary following a cue input.

(f) STOP ON CUE

The "Stop On" cue should be triggered during the last frame to be recorded. Cue 10 ("Recording") will open during the first field of the next frame.

(g) PLAY ON CUE

On pressing "Go" in the player, the first frame of the output clip is transferred to Harry's output.

Cue 12 ("Playing") will close after the first field boundary following an input cue. The frame following the one in which cue 12 closes will be the second frame of the clip.

(h) FEEDBACK

The cues which cause Harry to record are the same in the Feedback menu as in the Record menu. The output cues from Harry in the feedback menu are influenced by three parameters; "Input Fields/Input Frames", "Video Delay" and "Control Delay".

When Input Fields is selected, Output Cue 12 changes state twice for each output frame of video. When Input Frames is selected, Output Cue 12 changes once for each output frame.

Video Delay and Control Delay, when in Feedback mode, operate the following schedules.

INPUT FIELDS
Fetch frame to be processed from disks (takes 9-11 frames),
Frame on output of Harry- Cue 12 changes state,
Wait for Video Delay or Control Delay, whichever is greater,
Record first field at Harry's input,
Cue 12 changes state,
Wait for Control Delay (minimum 1 field),
Record second field at Harry's input,
Take next frame, until clip is finished (fetch frame only takes 2 frames).

INPUT FRAMES
Fetch frame to be processed from disks (takes 9-11 frames),
Frame on output of Harry- Cue 12 changes state,
Wait for Video Delay or Control Delay, whichever is greater,
Record frame at Harry's input,
Take next frame, until clip is finished (fetch frame only takes 2 frames).

2:5:4 Electrical Supply Connections

The Harry unit, the Disc Drives and control system have separate electrical supplies, which require the following:

The Harry Unit	1.8KVA (approx)
Each Disc Drive Unit	1.0KVA (approx)
The Control System	0.1KVA (approx)

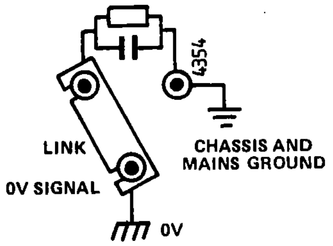
WARNING: The mains voltage cables for the PTD Disc Drives have the American standard colours: LIVE [Black], NEUTRAL [White] and EARTH [Green].

Caution: Ensure that each unit has the correct operating voltage before turning on !

2:5:5 System Earthing

To prevent earth loops, ensure that all earthing links within the system are set in the same position. The Earth selector link is situated on the rear panels of the Harry, Encore and Paintbox units, and is normally set in the Static Earth position shown.

Figure 2.5.4



WARNING: THE EQUIPMENT MUST BE EARTHED AT ALL TIMES !

2:5:6 Time Code Connections

This is a 3-pin XLR connector which is used to input a Longitudinal Time Code signal to the Harry system. The Time Code input is a balanced pair, which also can be used un-balanced by taking either pin 2 or 3 to ground. The amplitude of the analogue Time code signal should be stable within the amplitude range of 0.55 volts pk-pk to 10 volts pk-pk. The input impedance of the Time Code input is approximately 10,000 ohms

Note: the polarity of the balanced pair is not critical, as the transitions of the Time Code are decoded by the Time Code card.

XLR pin 1	Time Code
XLR pin 2	Time Code
XLR pin 3	Screen

This input is a conventional LTC audio input. Assuming the Time Code card 17724 is fitted, Harry can read both LTC (via this socket) and Vertical Interval Time Code (on the Coded input). SW1 on the Time Code card selects VITC or LTC operation.

2:5:7 Audio Input/Output

These are 3-pin XLR connectors which are used to input and output a standard audio signal to provide a low bandwidth scratch track. The audio input accepts a wide input signal amplitude range into a selectable input impedance of 150 Ohms, 200 Ohms, 620 Ohms or 50 KOhms.

The system's Audio Processor card processes the audio signal in digital form allowing up to 120 seconds to be stored in conjunction with a video clip.

XLR pin 1	Audio input/output
XLR pin 2	Audio input/output
XLR pin 3	Screen

2:5:8 Input/Output Panel Connections

The I/O Panel provides 4 digital Inputs and 4 digital Outputs. Two inputs and outputs are EBU 601 digital standard video connections and the other 2 Inputs and Outputs are Quantel standard digital video connections. These connections are used to interface to the system to other equipment with these standards. Note that Channel 4 is normally used as the connection to the Encore system.

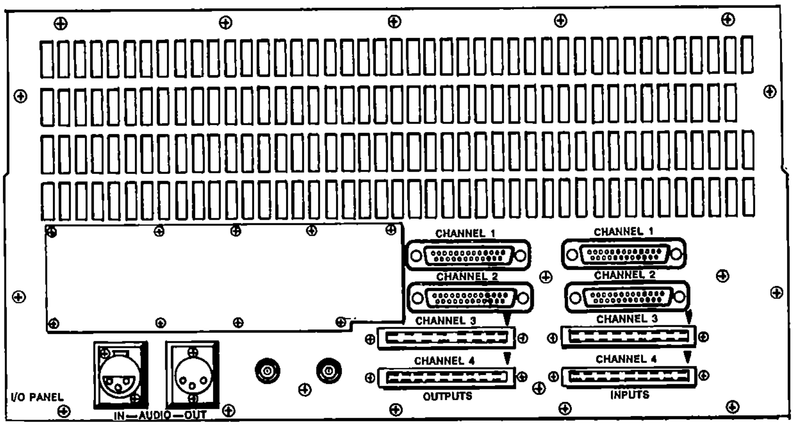


Figure 2.5.5 I/O Panel Connections

SECTION 6 : CONTROL SYSTEM INSTALLATION (2,6A)

2:6:1 General

The control system for Harry consists of a TDS Digitized Tablet (TDS LC-A3), a Pressure sensitive Pen and the Quantel keyboard. The connection between the control system and Harry is via an RS 422 serial link, which allows the user to operate the system remotely from the Harry unit.

2:6:2 Location

The Tablet should be situated away from stray magnetic fields and electro-magnetic interference. The control system requires a monitor to display the output of the Harry system, situated in the best position for the operator. see figure 2.6.1 for a typical control system layout.

2:6:3 Serial Link Connection

This connects from the 26-way D-type socket on the TDS Tablet to the 9-way D-type socket (TABLET) on the Harry unit. The serial Link can be operated with a maximum cable length of 300 Metres

2:6:4 Desk Mounting

The Tablet can be mounted on top of the Desk or flush with the desk surface. There are no fixing point to secure the Tablet to the Desk top and therefore Desks with steep inclines should be avoided, as the Tablet will only be held by the friction of the Tablet's feet.

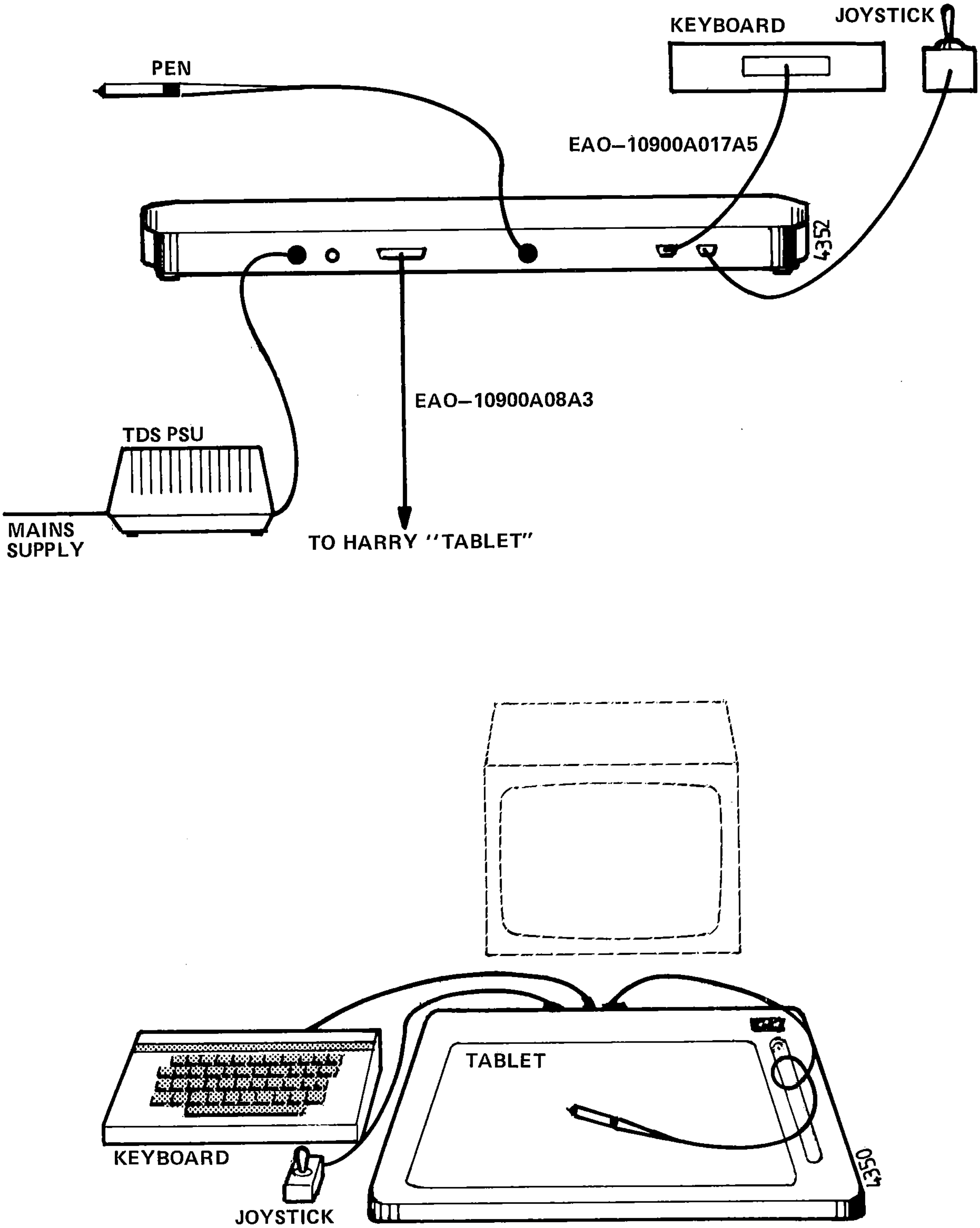
The Tablet can be mounted flush with the Desk top by cutting the Desk top to the shape of the Tablet and by securing the Tablet with brackets mounted to the underneath of the Desk. If the Tablet is to be mounted in this manner, then adequate air flow should be provided to cool the Tablet electronics and the PSU.

If the Tablet is to be Desk mounted, allow for easy access of the Tablet connectors and the other parts of the control station.

2:6:5 Multiple Control Stations

The control of the Harry system can only be shared between control stations by switching Stations to the "TABLET" input of the Harry unit. The Paintbox control, however can be switched from the Harry back to a separate Tablet by removing the "Paintbox-Artist cable (EA0 10900A008A6) from the "ARTIST" socket on the Paintbox, then connecting another Tablet to the "ARTIST" socket. This allows the Paintbox to be operated normally while the Harry system is used to edit. See Chapter 3 section 8 for cable and socket details.

FIGURE 2.6.1 CONTROL SYSTEM CONNECTION AND LAYOUT



SECTION 7 : SYSTEM CONFIGURATION

2:7:1 Coded RGB/YUV Options

(a) OPTIONS

The Harry system is supplied with Coded input and output facilities and can be expanded with the RGB/YUV input and output options. This option can be configured as RGB or YUV with links and Switch 1 on the RGB Input card. The configured option must be set as follows:

i. SWITCH 1 RGB INPUT CARD

UP	COMPUTER CONTROLLED
MIDDLE	RGB INPUT
DOWN	YUV INPUT

ii. SWITCH 1 RGB OUTPUT CARD

UP	COMPUTER CONTROLLED
MIDDLE	RGB OUTPUT
DOWN	YUV OUTPUT

(b) DECODER OPERATING MODES

The type of digital decoding process used within the Harry system can be selected on the Chroma Proc card. The system normally decodes the Coded input video using the "Adaptive Comb Filter" principle, but Comb and Simple decoding modes can be selected to suit certain types of Coded video signal.

i. SWITCH 1 NTSC CHROMA PROC CARD 17654

NORMAL	Adaptive Comb Filter Decoder
SIMPLE	Simple (Not Combed)
COMB	Comb Filter Only

ii. SWITCH 3 PAL CHROMA PROC CARD 17656

NORMAL	Adaptive Comb Filter Decoder
COMB	Comb Filter Only
SIMPLE	Simple (Not Combed)

iii. SWITCH 4 PAL CHROMA PROC CARD 17656

COMB ON	PAL Comb on giving Burst Phase correction
COMB OFF	PAL Comb off no Burst Phase correction

2:7:2 Computer Configuration

(a) CPU CARD CONFIGURATION

The rotary switches on the CPU card should be set to F (top switch) and 0 (bottom switch). These switches determine the source of the system operating software (F : RAM/ROM card). Note positions 0 to E on the CPU card top switch are not used.

(b) CIO CARD CONFIGURATION

The rotary switches on the CIO card determine the type of system and should be set to 0-NTSC or 8-PAL (top switch) and 0 (bottom switch).

2:7:3 Toggle Switch Positions

All Red front mounted toggle switches must be in the UP position for normal system operation, with the exception of those configuring RGB input and output functions.

2:7:4 Disc Drive Configuration

The Disc Drive units should have been correctly configured before shipment, but check using the information in this section. The Disc Drive configuration switches are situated behind the Disc Drive front panel. This hinged panel can be opened by loosening the locking screws on either side of the panel.

The four Disc Drive units are configured identically as follows:

(a) Spindle Remote/Local select	DOWN position
(b) CH 4/CH 5	DOWN position
(c) Rotation Ext A/Int/Ext B	UP position
(d) Enable/Disable A	UP position
(e) Enable/Disable B	DOWN position
(f) RLTM/ABSL	DOWN position
(g) MRTZ	DOWN position
(h) Drive Address	0000
(i) Sector Count	01001001-0101010
(j) Rotary Display Selection	Not "DIAG" position
(k) Numbered Switches	DOWN position
(l) Execute Switches	Do not Touch

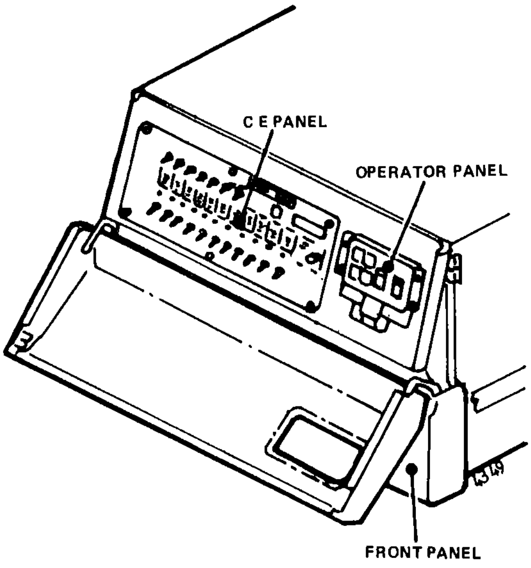
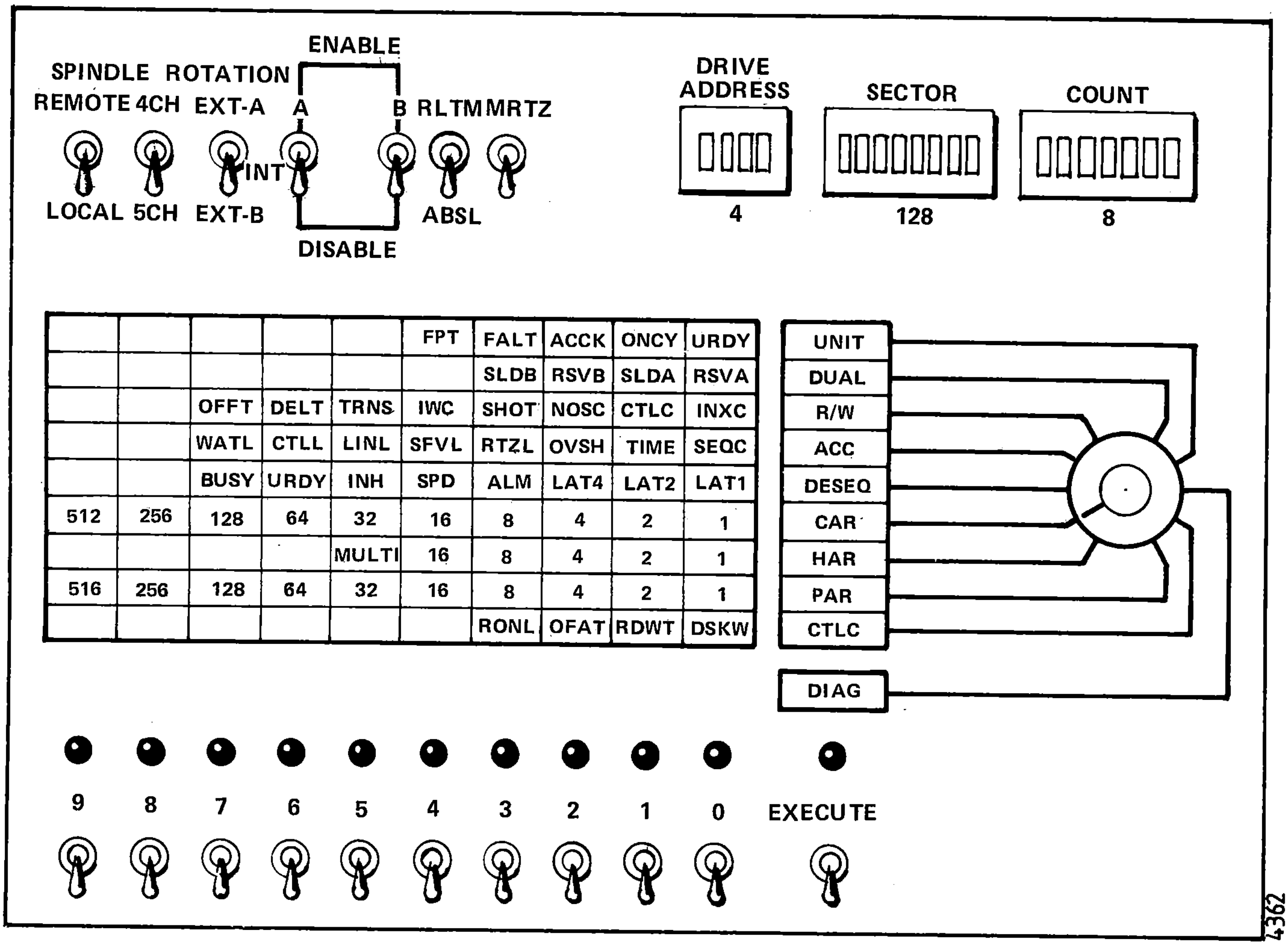


Figure 2.7.1 Disc Drive Configuration Panel

FIGURE 2.7.2 DISC DRIVE CONFIGURATION SWITCHES



					FPT	FALT	ACCK	ONCY	URDY
						SLDB	RSVB	SLDA	RSVA
		OFFT	DELT	TRNS	IWC	SHOT	NOSC	CTLC	INXC
		WATL	CTLL	LINL	SFVL	RTZL	OVSH	TIME	SEQC
		BUSY	URDY	INH	SPD	ALM	LAT4	LAT2	LAT1
512	256	128	64	32	16	8	4	2	1
				MULTI	16	8	4	2	1
516	256	128	64	32	16	8	4	2	1
						RONL	OFAT	RDWT	DSKW

SECTION 8 : SYSTEM STARTUP

2:8:1 General

On system power up or reset, the system computer (CPU, CIO and RAM/ROM cards) loads the system operating software from the RAM/ROM card into the RAM on the CPU card. When the system software has been loaded, the system computer initializes all of the system variables and runs through a "Self Test" routine before building the Menu display.

2:8:2 Normal Operation

For normal system operation the system switches should be configured as described in section 7 of this chapter.

2:8:3 Reset Modes

The system can be "RESET" (reload software and initialize system) in the following ways:

(a) By system power off and on.

(b) By pressing the RESET button (RED) on the CPU card.

(c) By software failure.

2:8:4 System Software Options

The system software can operate in a number of control modes, designated by the rotary switches on the CIO card. To obtain these different modes, it is necessary to set the Top rotary switch on the CIO card to the appropriate position and to reset the system. The following table gives information on the various settings:

0	NTSC system operating software.(Normal NTSC)
1	Development purposes only.
2	Not used.
4	Disables Auto start.
8	PAL system operating software.(Normal PAL)

2:8:5 Checking Correct System Operation

When the system is turned on the system computer runs a Self Test routine which checks the integrity of the Disc Controller cards Micro Code program and the Combiner cards RAM. Should a fault be detected the Harry menu will display an error message; giving the location of the detected fault. When the Self Test routine has completed, the following checks can be made to check the correct system operation.

(a) LIVE VIDEO PATH

From the top level menu select *Misc* then *Eng Setup.* Select Coded input video and using a suitable moving live source check that Harry system allows the video through to the Coded output.

Check also that the RGB inputs operate correctly and that Digital Colour Bars can be displayed successfully.

Return to the top level menu by using *End Setup.*

(b) DISC PATHS

From the top level menu select *IN/OUT* then *Record* and use the Pressure sensitive Pen to record a clip. To check that the Clip has been successfully recorded use *View* and the cursors on the View menu.

Check the Disc paths using the Digitally generated Test signals under the Misc menu.

Use the Library Menu to check that the Recorded clip can be saved in the Library and recalled correctly.

Note: If the Harry Menu displays "0 Frames Free", when recording a clip, this probably means that the Disc Drives connected to the system are initialized. To allow a clip to be recorded, the Directory entry for the Initialized Frames must be Deleted. This can be done by entering the Library Menu and then deleting the appropriate directory entry.

SECTION 9 : SYSTEM TIMING & ENGINEERING SETUP (2,9A)

2:9:1 **General**

(a) ENGINEERING ADJUSTMENTS

All Harry system timing adjustments and engineering functions are controlled from the control system Menu display. When timing the Harry system to the studio, always align the video outputs of the Harry unit to the Studio. The video outputs from a Paintbox, connected to Harry, may not be correctly aligned, and therefore should only be used as monitor outputs, as they do not represent the Harry system's output video.

(b) PRESET ADJUSTMENTS

The Harry system has a number of preset adjustments in the analogue video path which are critical and should only be changed when necessary. These preset adjustments should be adjusted as described in the system setup procedure. See chapter 3 section 4 for details.

Caution: All front mounted preset controls should not be adjusted out of sequence as this may adversely affect picture quality.

2:9:2 **Adjusting Engineering Values**

The engineering values are controlled by the control system and the Harry Menu display. Up to 8 different engineering set-ups can be stored and recalled to suit the needs of different studios. Note that on system power up or reset the values from file 1 are loaded. The engineering values are accessed via the menu display of the Harry system.

(a) ADJUSTING VALUES

The Engineering functions are within the *MISC* menu under *ENG SETUP*. Select the *ENG SETUP* for the engineering values menu and the menu display should show the engineering adjustments available. These will differ depending on which type of video source is selected.

Locate the value that is to be changed using the Pen cursor, and then use the keyboard to set the numeric value or the joy stick to increment and decrement the value.

(b) RECORDING VALUES

The Control system adjusts the values as they are set. If they are to be used again, they can be stored. Define a file number (1 to 8) with the keyboard, and record the engineering values displayed by using *SAVE SETUP*. The Menu display will report whether the file selected is already in use.

(c) RECALL VALUES

To access and use previously recorded engineering files, define the file number using the keyboard then *GET SETUP*. Note that the engineering files default to nominal values should the RAM/ROM card battery backup fail.

2:9:3 Harry Engineering Adjustments

Virtually all system alignments can be done using the engineering functions described in the following text. The system operating instructions give full details of the use of engineering functions.

(a) BLACK LEVEL

This controls the input video picture black level: Luminance - Coded, RGB and Component

(b) GAIN

This controls the input video gain: Composite - Coded, Luminance - RGB and Luminance - Component.

(c) HUE

This controls the input video HUE: Coded NTSC.

(d) BURST PHASE

Set for maximum vector amplitude: Coded PAL.

(e) O/P H PHASE

This controls the output video horizontal phase w.r.t. the output reference locking video: Coded, RGB and Component.

(f) O/P S PHASE

This controls the output video subcarrier phase w.r.t. the output reference locking video: Coded.

(g) I/P H PHASE

This controls the input picture phase w.r.t. the input locking video: Coded, RGB and Component.

SECTION 10 : SYSTEM INTERFACING

2:10:1 Connecting Encore To Harry

The Quantel DPE 5800/1 Encore system can be connected, digitally, to the Harry system, This allows processing of digital video from the Harry system using the Encore production effects system.

The Encore unit is accessed under *ENCORE* within the *FEED BACK* menu of the Harry control system.

2:10:2 Connecting Paintbox to Harry

A standard DPB 7000/1 Paintbox system can be modified to connect digitally to the Harry system. This allows Full Frame cell animation or Rotoscope effects to be produced on the Harry system. Details of the modifications required for the Paintbox are covered in a separate document. The external connections of a Paintbox to the Harry system are given in section 5 of this chapter.

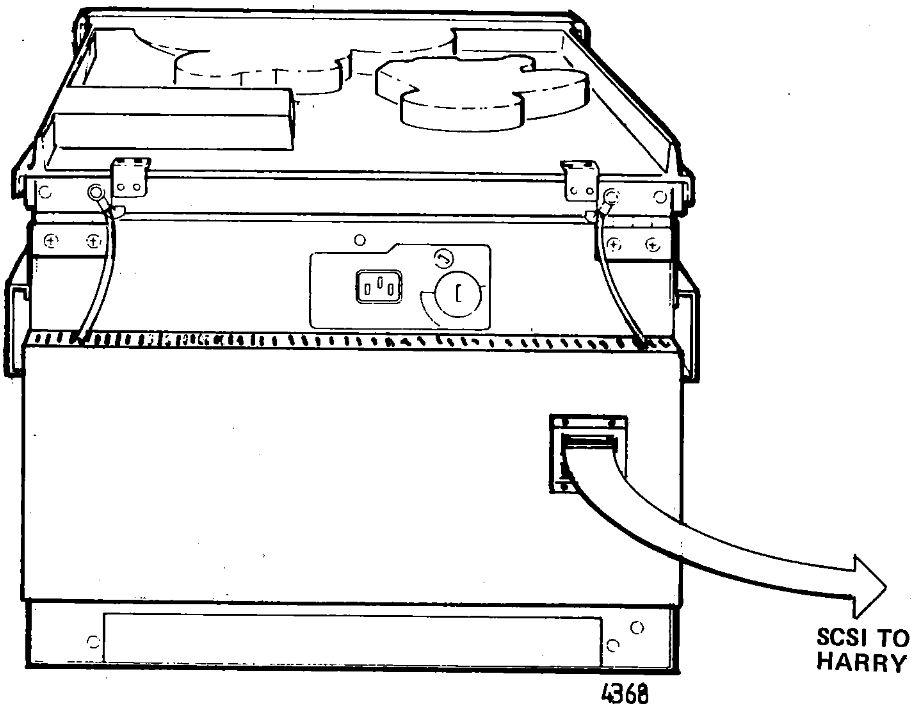
When a Paintbox is connected to the Harry system the video outputs on the Paintbox can only be used as monitor outputs, as the system is internally timed for the correct operation of the Harry system inputs and outputs. This does not, however, prevent modification of Harry Frames when the Paintbox is disconnected.

2:10:3 Connecting Magnetic Tape Streamer to Harry

The CIPHER M990 GCR Magnetic Tape unit can be connected to the Harry system to provide picture backup for archiving or bulk storage. The CIPHER unit is connected directly to the COMP SCSI socket on the rear of the Harry unit. The SCSI cable from the Harry rear panel connects to the Magnetic Tape unit as shown if figure 2.10.1.

The Magnetic Tape unit is accessed via the *TAPE SAVE* and *TAPE FETCH* menus. See operating instructions for full details.

FIGURE 2.10.1 SCSI CONNECTION



M990 GCR MAGNETIC TAPE UNIT

DCR 7700/1 HARRY
INSTALLATION AND SERVICE MANUAL
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SECTION 1 : GENERAL

3:1:1 Introduction

This chapter covers the maintenance and servicing of the Harry system. A complete system overview is given with guide lines on how to use the in built diagnosis and test facilities.

When carrying out Harry system maintenance the following should be remembered:

Caution: Always turn off the Harry unit before removing or inserting PCBs into the unit, to prevent damage to the edge connector pins and the electronic circuitry on the PCBs.

Caution: Beware of oscilloscope probe earths when investigating cards as there are power rail fuses on each PCB fitted to protect the PCB and the Highway should a fault occur.

DO NOT, under any circumstances link out these fuses because the System PSU is capable of delivering 200 Amps of +5 volts.

WARNING: Always disconnect the Harry system from its electrical supply before attempting to remove or insert the Power supply unit or any of the unit panels because dangerous voltages can be exposed.

WARNING: The fans within the Harry unit continue to rotate for a period of time after the electrical supply has been removed.

WARNING: Always ensure that an adequate number of persons are available when the Disk Drives or the Crate and Power supply units are being lifted. See handling instructions in chapter 2.

WARNING: NEVER HAVE MORE THAN ONE UNIT ON EXTENDED SLIDES, AS THIS MAY CAUSE THE CABINET TO FALL OVER.

3:1:2 Static Damage

Caution: The Integrated Circuits and other components fitted on printed circuit boards in the system units can be irreparably damaged if static discharge occurs.

To a certain extent nearly all components can be damaged by static discharge and static fields. Therefore adequate precautions must be taken to prevent any possible damage.

Static damage is unlikely to occur when the printed circuit boards are fitted as the PCBs provide local earth plains, but this may not protect devices should the PCBs be removed from the units.

Note: If component replacement is to be carried out, ensure that this is done in a static free area.

3:1:3 Printed Circuit Boards

(a) GENERAL

The printed circuit boards that are mounted in the front of the crate assembly have designated power supply rails, which are present in each card slot. The power rails used on each card are shown on the circuit diagram for the card. Pin 6 of the edge connector is a key way which prevents mechanical misalignment of the cards. This however does not prevent cards being situated in the wrong card slots.

The component side of the printed circuit is designated as the "A" side of the card and the track side the "B" side. Each pin of the edge connector on the card has a number and the letter A or B determining the side of the connector. The top pin on the edge connector (as inserted in the crate assembly) is pin 1.

(b) HIGH INSERTION EDGE CONNECTORS

The Printed Circuit Boards are fitted into the crate assembly with High-Insertion edge connectors. These connectors have a limited insertion life, and therefore PCBs should not be removed and inserted on a regular basis as this may affect the reliability of the connections.

The Gold edge pins on the Pcbs should not be touched by hand because residue from the fingers may corrode the surface of the pins, making the connections unreliable. If the Gold pins are touched they should be cleaned with an alcohol wipe.

(c) IC SOCKETS

The IC sockets used within the system are High-Insertion and therefore care should be taken when removing and inserting ICs or programmed devices to avoid damage to the sockets or devices. Note that the correct IC removal tool should be used at all times to avoid stressing the device.

(d) PCB TYPE NUMBERS

Each Printed Circuit Board is numbered with the board type, the PCB artwork issue letter and the Modification Status number of the PCB assembly. The PCB type and issue are usually placed by the front edge of the card so that they can be read without removing the card, but this is not always the case.

3:1:4 Using Extender Boards

Ensure that the system's power has been turned off before an Extender card is plugged into the crate or a PCB is plugged into the Extender card, as misalignment of the edge pins will cause damage if the system is on. When a Printed Circuit Board is to be plugged into the Extender card, care must be taken to ensure that the PCB does not fall from the Extender card's edge connector.

SECTION 2 : SYSTEM OVERVIEW

3:2:1 Input Section

(a) COMB DECODER

The Coded input video from the rear panel is passed to the ADC card where it is clamped and separated into LF Luminance and HF Luminance + Chrominance signals prior to digitizing. This digital video is passed through a set of 1H delay lines which provide the appropriately delayed data required by the Chroma Processor card Comb filter circuit.

The Chroma Processor card Combs the early, middle and late HF+CHR, and the middle LF, to produce wide band Luminance (Y) and pure Chrominance. This Chrominance is synchronously quadrature demodulated by the U' and V' subcarriers from the Input Timing card. Then the base band U and V subsequently produced are then passed to the Filter card where unwanted frequency components are attenuated.

(b) DATA PATHS

The filtered U and V data is co-site sampled and multiplexed then passed to the Input Switch card timed with the Y data from the Chroma Processor card. The Input Switch card selects the appropriate source of Y and U/V data and passes the data to the appropriate Mux Demux card (Y to Top rack card and U/V to Bottom rack card) and the I/O Store.

(c) I/O EXPANDER INPUT

The I/O Expander Input card mounted in the rear of the unit allows the selection of 4 digital video inputs, 2 EBU 601 and 2 Quantel digital inputs. The Y, U/V and Key data from the selected input (Channel 1-4) is demultiplexed by the card and passed to the Chroma Proc, where it can be routed to the Input Switch card.

The Y and U/V data from the Paintbox is passed via the Input A connection into the Codec card, where they are routed to the Input Switch card.

(d) INPUT TIMING

Input timing and clock signals for the system are generated by the Input Timing card and are phase locked to the input locking reference video. Syncs are stripped from the Coded input video or from the RGB Sync input and the 13.5MHz input system clock is phased locked to the leading edge of the reference syncs.

The Digital U and V subcarriers, required by the Chroma Processor card to demodulate the input Chrominance, are produced by the Input Timing card. They are generated at 13.5MHz sampling rate and are phase locked to the input locking reference burst.

3:2:2 Satellites

(a) STRUCTURE

There are four identical Satellite sections within the system, which consist of a Buffer Store section, a Combiner section and a Disk Interface section. The Satellites are controlled by the system computer and all operate in parallel on the four components of the Video:

Y1 - Top Left Satellite
Y2 - Top Right Satellite

U - Bottom Left Satellite
V - Bottom Right Satellite

(b) TYPICAL WRITE PATH

The Y data from the Input Switch card is separated into alternate samples of Y1 and Y2 data. These are passed to the Top Left and Top Right channels respectively. The U/V data from the Input Switch card is separated into alternate samples of U and V data, which are passed to the Bottom Left and Bottom Right channels respectively.

The data in each of the four channels is passed through the appropriate channel Data Select card, and written into the Satellite Store, controlled by the Store Address card.

The channel data from each of the Satellite Stores is Read out and passed to the Data Select card, controlled by the Store Address card, then buffered by the Disk Interface card. The data is then written onto the appropriate Disk Drive unit, controlled by the channel's Disk Controller card.

(c) TYPICAL READ PATH

Data read from the four Disk Drive units is buffered by the Disk Interface cards, under the control of the channels' Disk Controller cards. The data is then passed through the Data Select cards and written into the Satellite Stores, under the control of the channels' Store Address cards.

The Satellite store is read and the data is passed through the Data Select cards into the appropriate Mux/Demux card, controlled by the Store Address cards.

The Y1 and Y2 data from the TL and TR Discs are multiplexed by the top rack Mux/Demux card to produce continuous Y data. The U and V data from the BL and BR Discs are multiplexed in the bottom rack Mux/Demux card to produce U/V data. The Y and U/V data from the Mux/Demux cards is then passed to the Input Switch card and then written into the I/O Store.

(d) COMBINER

The Combiner card in each satellite is used to process frames of video data held in the Satellite Stores. All processing is carried out while data is being transferred from Buffer to Buffer, controlled by the system computer.

Typically, two different Frames of data are read from 2 separate Buffers (example A and D), processed with a key from a third buffer (from another satellite via the combiner bus), then written back via an empty buffer onto Disk.

(e) DISK ACCESS

The Parallel Transfer Drives (PTD) used by the system are controlled by the Disk Controller card via the four individual "Bus" connections.

Data is transferred, via the four individual "Radial" connections, in 5 serial lines which correspond to the Disks' 5 parallel heads. Conversion between this format and the 8-bit parallel format used throughout the system is carried out by the Disk Interface card.

3:2:3 Output Section

(a) CODER

The Y and U/V data from the I/O Store is passed to the Coder card, where the Y data is blanked and has syncs added before it is converted to analogue. The U/V data is blanked and has burst added before it is modulated by the U' and V' subcarrier data from the Output Timing card. The modulated Chrominance data is converted to analogue and added to the analogue Luminance.

The Y and U/V data from the I/O Store are also passed to the RGB Output card, where they are blanked and converted into analogue Red, Green and Blue signals. The Y and U/V data is routed through the Codec card to be passed to the Paintbox Input side via the Output A connection.

(b) I/O EXPANDER OUTPUT

The Luminance (Y) data, the Chrominance (U/V) data and key data generated by the Coder card are passed to the I/O Expander card mounted in the rear of the unit. The data is formatted into 2 Quantel digital outputs and 2 EBU 601 outputs for connection of the system into the Digital Production Centre (DPC) and the Digital Studio.

(c) OUTPUT TIMING

Output timing and clock signals required by the system are generated by the Output Timing card and are phase locked to the output locking reference video. Syncs are stripped from the output referenced video, then the 13.5MHz output system clock is phased locked to the leading edge of the reference syncs.

The Digital U and V subcarriers, required by the Coder card, are produced by the Output Timing card. They are generated at 13.5MHz sampling rate and are phase locked to the output locking reference burst.

3:2:4 Time Code & Cues

The system accepts and generates cue signals, which are used to interface the system with other equipment. The system also decodes EBU standard Longitudinal Time Code (LTC) and Vertical Interval Time Code (VITC) so that Match-Frame editing can be performed. These functions are controlled by the Time Code card in conjunction with the system computer.

3:2:5 Audio

The system can provide a low bandwidth Audio Scratch-track which can be used to store an audio signal in conjunction with a recorded video clip. The Scratch Track is provided by the Audio Processor card, which is controlled directly by the system computer.

3:2:6 System Control

The Harry system is controlled and interrogated by the system computer, which consists of the CPU card, the CIO card and the RAM/ROM card. This computer interfaces the control station to the Harry unit, provides all internal control of the Harry unit and also controls the Paintbox facilities of the Harry system.

The system computer bus is a multiplexed 16-bit Address/Data bus. This bus is passed along the two card card Highways with 3 bus control signals; STROBEL which clocks data on and off the system bus, READL which determines whether the system bus is to read from or written onto, and ADDRL which determines whether there is an Address or Data on the system bus.

The system is memory mapped, with each card responding to specific address locations within the memory map. Each card holds bus decoding circuitry which determines when data on the system bus is to be used by the particular card. The STROBEL signal clocks data from the system bus into the selected register on the addressed card. These computer loaded registers are used to hold system variables and to control the functions performed by the cards.

3:2:7 Paintbox

(a) STRUCTURE

Picture transfer between the Paintbox system and Harry system is controlled by the Harry system computer and achieved by routing data via the Codec and the Harry Interface cards. The Paintbox is controlled by the Harry system via serial connections which connect together the two system computers, allowing control from the single Tablet control station.

(b) TIMING

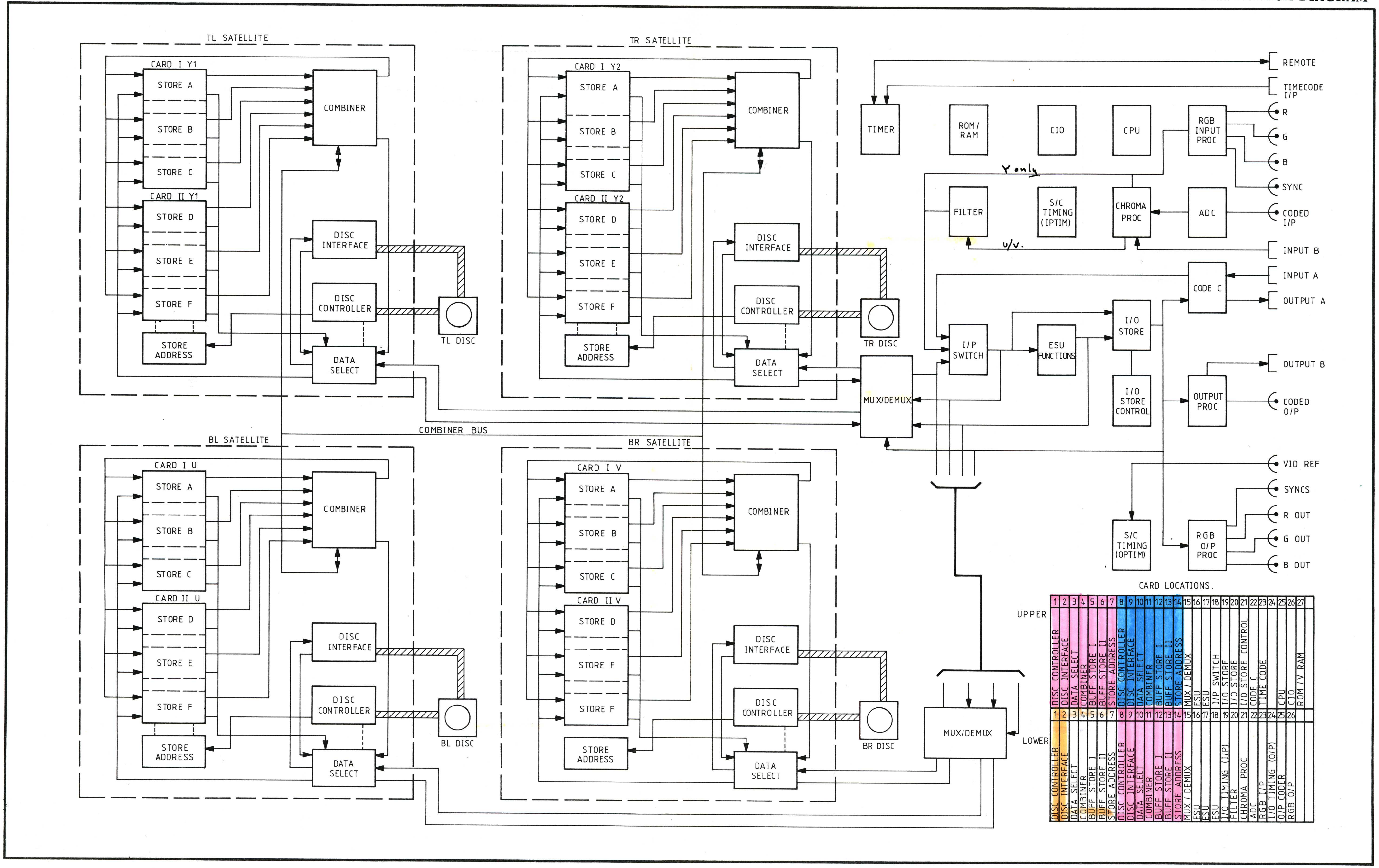
When a Paintbox is connected to the Harry system, timing signals and clocks are generated locally at the source of the digital video. These are routed between the Paintbox and Harry via the Codec and the Harry Interface cards.

(c) DATA PATHS

The Y and U/V data generated by the Harry system are buffered by the Codec card and transferred via the Output A connection to the Harry Interface card in the Paintbox. The data is then passed to the Paintbox Input Timing card for processing by the Paintbox.

The Y and U/V data generated by the Paintbox system Combiner card are passed to the Harry Interface card, where they are buffered before being transferred via the Input A connection to the Codec card.

(3,2B)
FIGURE 3.2.1 SYSTEM BLOCK DIAGRAM

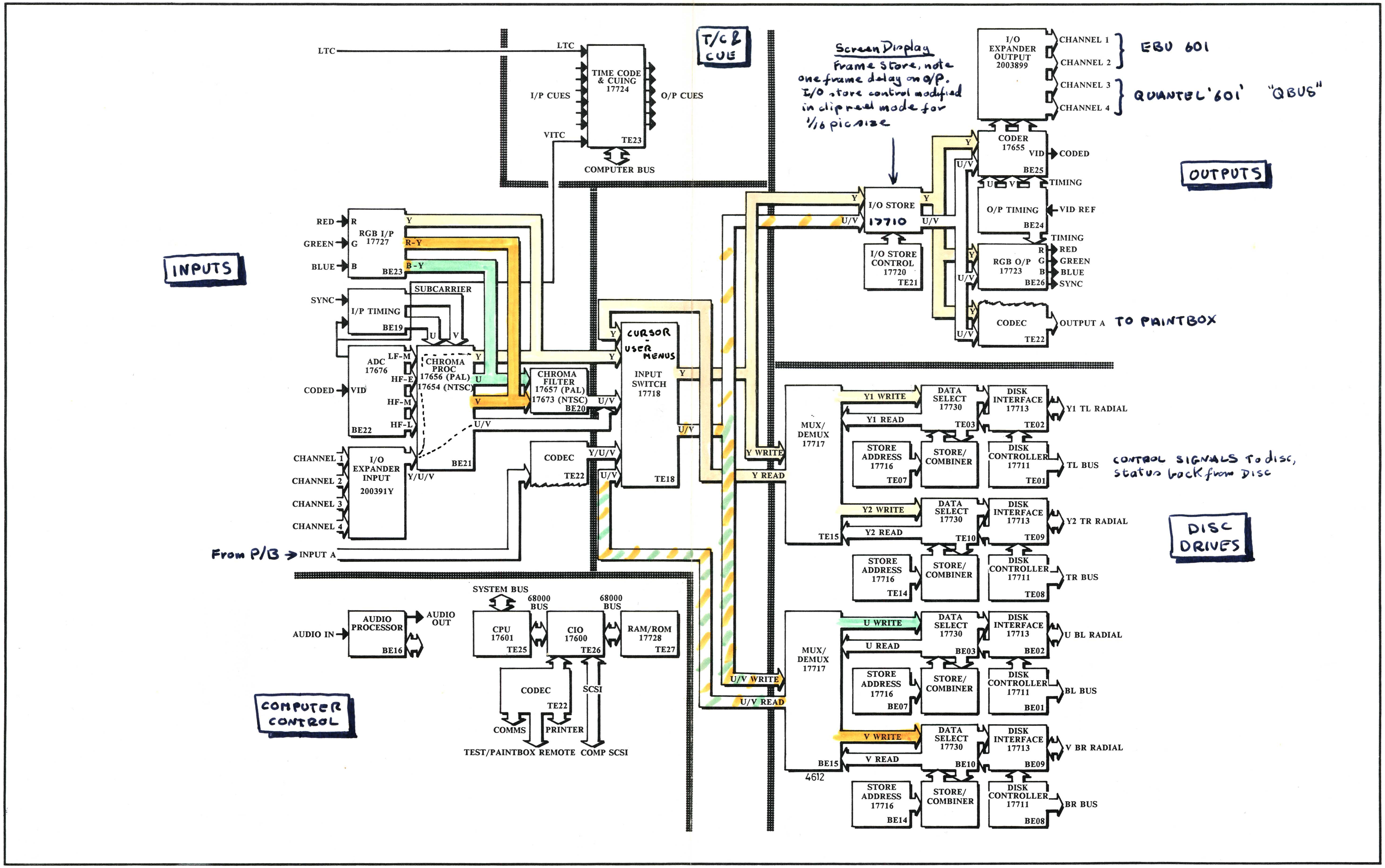


CARD LOCATIONS.

	UPPER	LOWER
1	DISC CONTROLLER	DISC CONTROLLER
2	DISC INTERFACE	DISC INTERFACE
3	DATA SELECT	DATA SELECT
4	COMBINER	COMBINER
5	BUFF STORE I	BUFF STORE I
6	BUFF STORE II	BUFF STORE II
7	STORE ADDRESS	STORE ADDRESS
8	DISC CONTROLLER	DISC CONTROLLER
9	DISC INTERFACE	DISC INTERFACE
10	DATA SELECT	DATA SELECT
11	COMBINER	COMBINER
12	BUFF STORE I	BUFF STORE I
13	BUFF STORE II	BUFF STORE II
14	STORE ADDRESS	STORE ADDRESS
15	MUX / DEMUX	MUX / DEMUX
16	ESU	ESU
17	ESU	ESU
18	I/P SWITCH	ESU
19	I/O STORE	I/O TIMING (I/P)
20	I/O STORE	FILTER
21	I/O STORE CONTROL	CHROMA PROC
22	CODE C	ADC
23	TIME CODE	RGB I/P
24		I/O TIMING (O/P)
25	CPU	O/P CODER
26	CIO	RGB O/P
27	ROM / V RAM	

(3,2B)

FIGURE 3.2.2 SIMPLIFIED BLOCK DIAGRAM



3:2:8 Board Functions

(a) RGB INPUT CARD

The function of this card is to buffer, black level clamp and digitize the Red, Green and Blue input signals, then Matrix them to produce Y and U/V data for the system. This card is configured for RGB or YUV input signals.

(b) ADC CARD

The main function of this card is to buffer, black level clamp then separate the input Coded video signal into LF Luminance, and HF Luminance plus Chrominance data. This data is required by the Chroma Processor card to Comb filter and decode the Coded video.

The ADC card also provides digital Coded test videos which can be used to prove the correct operation of various cards in the system.

(c) CHROMA PROC CARD

This card in conjunction with the ADC card forms the "Adaptive Comb Filter" and decoder of the system. This produces wide-band combed Luminance, and demodulated "U" and "V" components.

The Chroma Proc card accepts Middle-LF Luminance (1H delayed), and Early, Middle and Late-HF Luminance + Chrominance. The Input Timing card provides data used to produce digital U and V subcarriers; which demodulate the Combed Chrominance data to produce U and V base data.

(d) CHROMA FILTER CARD

The function of this card is to remove any unwanted frequency components, from the U and V base band data, produced by the demodulation process carried out on the Chroma Processor card.

The card consists of two identical Finite Impulse Response filter circuits; one for U and one for V. The filtered U and V data produced, are range-limited, multiplexed together and then passed to the Input Switch card.

(e) INPUT SWITCH CARD

This card has the following functions; to select Live, Digital or Satellite data for processing; to Interpolate data before it is compressed into the I/O Store; to provide the Menu Cursor.

The Input Switch card also holds a computer timing signal generator circuit, which is used to write the user menu into the I/O Store.

(f) MUX/DEMUX CARD

The function of each Mux Demux card is to multiplex the data from two satellites (U and V in the bottom rack or Y1 and Y2 in the top rack) when data is read from these Discs, and to de-multiplex the Luminance or U/V when data is to be written into the four satellites from the Input Switch card.

(g) DATA SELECT CARD

There are 4 Data Select cards in the system; one in each satellite. The function of these cards is select data from the Mux Demux cards, the Disk Interface cards, the Combiner cards and the Buffer Stores, then pass the selected data to the Buffer Store, the I/O Store or Disk Interface cards.

This card also holds circuitry used to generate Crop windows so that selected sections of the Buffer Store can be written.

(h) DISK INTERFACE CARD

There are four Disk Interface cards in the system; one for each Disk Drive. Each Disk Interface card interfaces the parallel 8-bit data format used in the satellites with the 5 serial data paths provided by a specific Disk Drive.

The function of this card is to interface the Disk drive data path with the system. The system provides data in 8-bit word format which has to be converted into 5 serial data streams which correspond directly with the 5 parallel Heads on the the PTD Disk Drive.

(i) DISK CONTROLLER CARD

The function of this card is to convert instructions from the system computer into Disk control information. This card uses a bit slice sequencing element to provide the addresses for a 64-bit wide micro code word held in RAM on the card. This micro code word controls the operation of the Disk Drive; setting up the Disk when data transfer between the Disk and the system is required.

(j) BUFFER STORE CARD

The function of the Buffer Store is to hold satellite data while it is being written into or read from the satellite Disk Drive. The store consists of two Buffer Store cards each holding 3 Buffers: A, B and C which have 4 store stripes.

Data is written to a buffer on one video Frame then read out during a later video Frame.

(k) STORE ADDRESS CARD

The function of this card is to provide the Read and Write addresses for the satellite Buffer cards. The addresses control the writing data to and reading data from the Disk. The Store Address card consists of two similar address generator circuits which can be used for either read or write addressing. Although for nearly all operations the two circuits are dedicated to one function.

(l) COMBINER CARD

There are 4 Combiner cards in the system, one in each satellite. The function of this card is to combine selected data from the system to produce dissolves, temporal filtering, Luminance keying, mixing and other effects. The Combiner has two channels A and B which are used to process two selected video sources and one channel C for keying from eight possible input sources.

(m) I/O STORE CARD

The I/O Store is a video Framestore which is used to store and display the system's video output and menu display. The Store consists of two cards; one for Luminance data and the other for U/V data.

Video data selected by the Input Switch card is stored in the I/O Store, controlled by the I/O Store Control card, and provides a full Frame of Luminance and U/V data for the Output Proc and RGB Output Proc cards.

(n) I/O STORE CONTROL CARD

The function of this card is to produce the addresses, strobes and enable signals for the I/O Store. This card has two address generator circuits which produce independent Read and Write addresses.

(o) CODER CARD

The main function of this card is to take the Luminance and U/V data from the Output Store, and to digitally Encode them to produce the analogue Coded video output.

The U/V data from the I/O Store is de-multiplexed and digitally blanked before having burst added. The "U" and "V" are then modulated with digital subcarrier data from the Output Timing card. The Chrominance components are added together and then the Chrominance data is converted to analogue.

The Luminance data from the I/O Store is digitally blanked and has sync pulses added prior to conversion to analogue. The analogue Luminance and the analogue Chrominance signals are then summed to produce the composite Coded Output signal.

(p) RGB OUTPUT CARD

The function of this card is to matrix the YUV data from the I/O Store to produce RGB data. This data is converted to analogue, filtered, and passed from this card as the RGB output video signals. This card can also be configured to provide YUV output signals. Normally this card is configured for either RGB or YUV outputs.

(q) I/O TIMING CARD

There are two Timing cards within the system; one on the input (Write) side of the system and one on the output (Read) side of the system. Their function is to produce the necessary reference locked timing signals, and U and V subcarriers for the system.

(r) CODEC CARD

The function of this card is to provide the video data interface between the Harry and the Paintbox systems. This card provides Luminance and U/V data paths to and from the Paintbox and two sets of Horizontal and Vertical counters which time the Paintbox system to the Harry output reference video.

(s) CPU CARD

The CPU card, the CIO card and the RAM/ROM card form the Harry system computer. The CPU card is a 68010 based Micro Processor computer with a Floating Point processor. The card also carries various interfacing circuitry and the Micro Processor's memory. The system operating software is held in the RAM/ROM card and is loaded into the CPU Ram on power up or system Reset.

(t) CIO CARD

The CIO card performs four major functions within the system computer, in conjunction with the CPU card:

Serial Interfacing to external peripherals.

DMA control of data transfer between the system computer and peripherals.

SCSI interface.

VDU Graphics display. (not used)

(u) RAM/ROM CARD

The function of this card is to store the system operating software and to provide non-volatile RAM for storing system constants such as Engineering setups and Disk Directories.

This card can be configured to provide addressed areas of Eprom and Non volatile Static RAM. The card consists of the three blocks which are linked for Eprom or RAM use. Each Block is addressed from the system computer and accessed via the 68000 bus from the CPU card.

(v) TIME CODE CARD

The function of this card is to decode the Vertical Interval Time Code (VITC) and Longitudinal Time Code (LTC) to provide Match Frame editing facilities.

This card also provides output and input cue lines which enable the Harry system to cue external equipment and to be cued by 4 different external sources.

(w) AUDIO PROCESSOR CARD

The function of the Audio Processor card is to provide an audio scratch track for the system. This is used to store the audio track associated to a particular Video clip.

The card accepts a standard audio signal as its input, and provides an output signal synchronous with the processed output Video clip being generated. The card processes the audio signal in digital form, allowing up to 120 seconds to be stored in the 1 Mbit DRAM section on the card.

(x) I/O EXPANDER INPUT

The function of this card is to provide 4 selectable digital video inputs for the system, 2 EBU 601 digital inputs and 2 Quantel standard digital inputs. The card is mounted in the rear of the Harry crate assembly on the inside of the top rear panel (I/O Panel). The card forms a 4 - 1 selector, controlled by the system via the PAL HF.

(y) I/O EXPANDER OUTPUT

The function of this card is to provide 4 digital video outputs for the system, 2 EBU 601 digital outputs and 2 Quantel standard digital outputs. The card is mounted in the rear of the Harry crate assembly on the inside of the top rear panel (I/O Panel).

3:2:9 Control System

(a) GENERAL

When the Harry system is to be installed with an existing Paintbox system, the Tablet previously used by the Paintbox will be connected to the Harry system. The Tablet will then control both the Harry and the Paintbox. If the Harry system is to be used without direct connection to a Paintbox system, the Tablet will be supplied as part of the Harry system.

Two different Tablets can be used as the Harry system control station: the Sumagraphics controller and Tablet or the TDS Tablet.

(b) SUMAGRAPHICS TABLET & CONTROLLER

The Sumagraphics control system consists of a Tablet, Controller unit and a pressure sensitive Pen. The Sumagraphics Controller unit is modified for use with the Quantel Pressure sensitive Pen and keyboard. An interface card is built into the Controller unit which interfaces to the Harry system. For further information consult the Sumagraphics manual.

(c) TDS TABLET

The TDS control system consists of a Tablet, Power Supply and a Pressure sensitive pen. The TDS Tablet is modified for use with the Pressure sensitive pen and the Quantel Keyboard. An interface card is built into the Tablet which interfaces to the Harry system. For further information consult the TDS Tablet manual.

(d) TABLET OPERATION

The Tablet is address mapped to provide Horizontal (X) and Vertical (Y) coordinates; relating the position of the Pen on the Tablet surface with the position of the cursor on the menu display. The Pen transmits a signal, which is received by the Tablet to produce the X and Y positional coordinates. These directly relate to the X and Y picture point addresses of the I/O Store.

The pressure value produced by the Pen is monitored by the system computer and allows the section of specific menu options, when the Pen is pressed in the designated menu area of the Tablet/Menu display.

(e) SERIAL DATA TRANSMISSION

The Horizontal and Vertical Tablet coordinates and the Pen Pressure data produced by the Tablet system are transferred to the Harry unit in serial data packets. These data packets are produced by the Tablet Interface card mounted within the Tablet (TDS) or the ID20 Tablet Controller (Sumagraphics) and passed via the RS 422 serial link. The Tablet interface also encodes the Keyboard and Joystick data to produce serial data packets containing Keyboard and Joystick data.

3:2:10 Crate Mechanical Overview

The Harry crate assembly is constructed of a welded steel enclosure with compartments for the Power Supply Unit, the card frame and the Highway and back panels.

The crate assembly has been designed to provide easy access to all of the major system parts. The PSU is a separate removable unit; removed from the front of the crate assembly (see chapter 2 for details). The Highway can be accessed via the hinged back panels by removing the screws marked with the white arrows (figure 3.2.3) This hinged panel also gives access to the internally mounted printed circuit board and the internal wiring.

The top front panel of the crate assembly allows access to the Fan tray fitted in the top enclosure of the crate assembly.

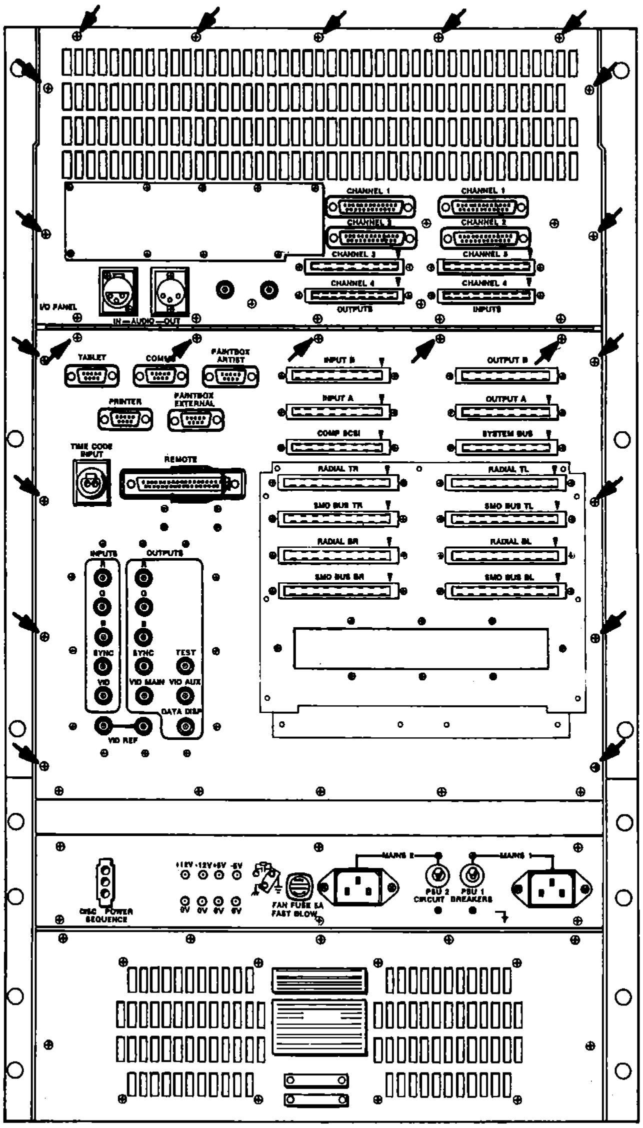


Figure 3.2.3 Access Through Hinged Rear Panels.

(3,2B)

The I/O Expander cards are mounted on the inside of the top rear panel. The can be accessed by removing the screws marked with white arrows as shown in figure 3.2.3. The two boards are mounted to the top rear panel as shown in figure 3.2.4.

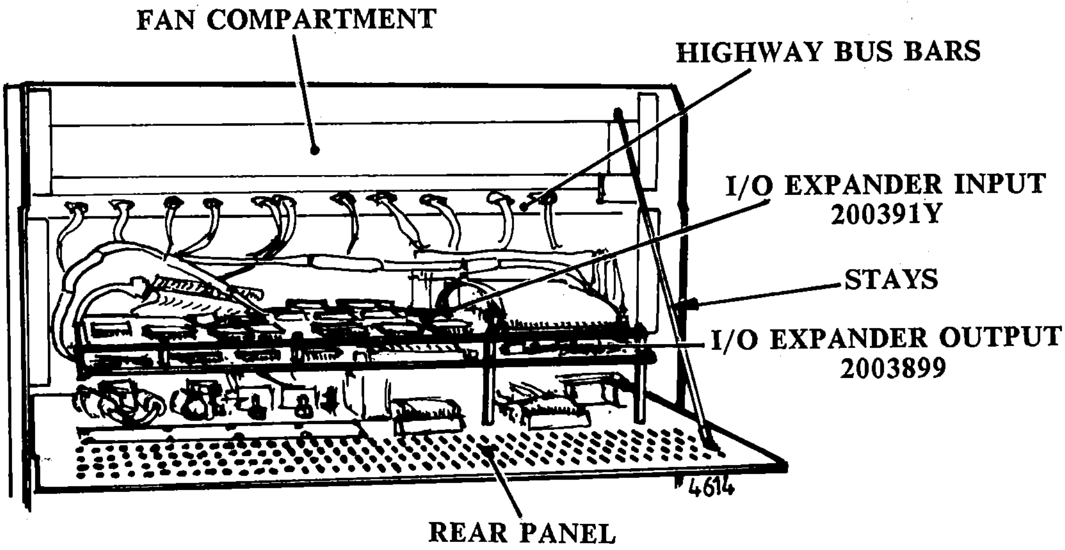


Figure 3.2.4 I/O Expander Boards

The Power Supply unit is cooled by air drawn through the PSU front panel, across the PSU module, through the rear mounted fan units and expelled at the rear of the PSU. The Printed circuit boards mounted in the front of the crate assembly are cooled by air drawn through the PSU front panel, between the PCBs, through the top mounted fan tray and expelled at the rear of the unit.

All video connections on the bottom rear panel are screened by the metal box, mounted on the inside of the panel, on which the Coax board is mounted.

3:2:11 PSU Assembly

The power supply unit is constructed of a welded steel tray with two compartments, separated by two formed plates which ensure that the PSU and the crate assembly are cooled front to back. One compartment in the PSU houses the fan units and the other houses the PSU modules and associated wiring. See figure 3.2.5 for construction details.

The system Power Supply unit consists of two Switch Mode PSU modules; the larger supplying the +5 volts (logic) and the smaller supplying the other system power rails.

The mains supply is switched to the PSU modules via the mains relays, which also switch the supply to the Fan units within the crate assembly. The mains relays are activated by the front mounted Power switch.

The Power supply unit is protected by over current trips on the electrical supply input, mounted at the rear of the unit and both PSU modules are internally protected by fuses.

The +5 volt (logic) PSU module provides only one adjustment (voltage output).

Caution: This which should not be adjusted unless absolutely necessary as the module can deliver 200 Amps at a voltage of greater than 5.2 volts. If the module output voltage is greater than +5.2 volts the reliability of the system may be adversely affected.

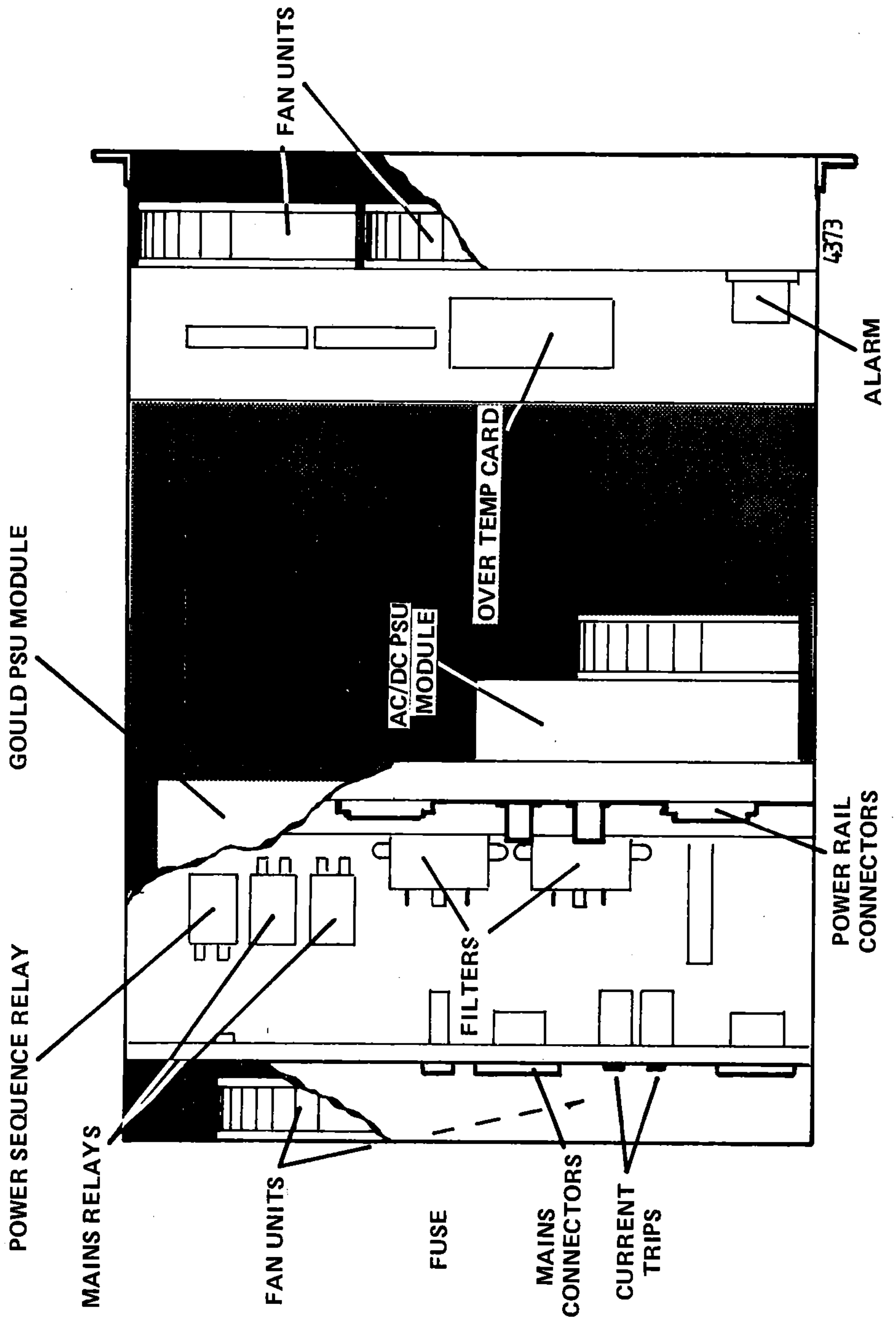
The power rails are tracked along the card Highway and connect to the Printed Circuit Boards via designated edge connector pins:

Edge pin	Voltage		Rating	PSU Module
AB1	0V	Logic		
AB2	0V	Logic		
AB3	+12V	Analogue	3 Amps	Gould
AB4				
AB5	+5V	Logic	200 Amps	AC DC
AB6		Key way		
AB7	-5V	Analogue	20 Amps	Gould
AB8				
AB9	-12V	Analogue	3 Amps	Gould
AB10	0V	Analogue		

The Power supply unit provide the Disk Power sequence output for the Disk Drives fitted to the Harry system, which ensures that the Disk Drives are powered up and down in the correct sequence.

The Power Supply unit houses the Over Temperature Alarm system which measures the internal air temperature in a number of places within the crate assembly, and sounds the front mounted alarm if the internal air temperature rises above the preset level.

FIGURE 3.2.5 POWER SUPPLY UNIT



SECTION 3 : ROUTINE MAINTENANCE

3:3:1 General

The Harry system requires minimal routine maintenance to aid its continual function. This section contains information relevant to routine system maintenance.

Because of the digital Coding and Decoding techniques used in the Harry system the analogue circuitry and therefore routine alignment has been reduced to a minimum. Under normal operating conditions the analogue circuitry should not drift, however, analogue adjustment may be required occasionally to compensate for component aging.

3:3:2 Video Alignment

Day to day "Proc amp" type adjustments can be carried out using the Engineering facilities of the Harry system (see chapter 2 section 8 system timing). If however, there is need to adjust the preset adjustments see section 4 of this chapter for the system alignment procedure.

3:3:3 Air Filters

The air filter for the Harry crate assembly is held in the front of the PSU front panel. This needs cleaning on a regular basis to prevent the system from over heating caused by reduced fan speeds.

Caution: Do not run the Harry system with the air filters removed as this may affect the reliability of the system.

The fan air filter in the PSU front panel should be removed, by sliding it from its retaining brackets, and cleaned using an Air Hose. See chapter 2 for details on removing the PSU front panel.

3:3:4 Pressure Sensitive Pen

The Pressure sensitive Pen used with the control system is a delicate device, and therefore great care must be taken to avoid damage when it is being used or when it is stored. The following guide lines should be remembered so that the full operational life of the Pen can be ensured:

i. Do not attempt to take the Pen apart, as this will perminantly damage the Pen

ii. There are no user adjustments on the Pen.

iii. Avoid using excessive pressure when using the Pen as this will stress the Pen and increase wear on the Tablet surface.

iv. Avoid heaving tapping of the Pen on the Tablet or any hard surface as this will cause damage to the delicate moving parts inside the Pen.

v. When the Pen is not in use for long periods, the Pen should be stored away from areas of strong light as this may cause the plastic to deteriorate and become brittle.

SECTION 4 : SYSTEM ALIGNMENT PROCEDURE

3:4:1 Video Alignment

(a) GENERAL

This section contains information relevant to the alignment of the Harry system analogue circuitry. The alignment procedures in this section should not be necessary on a routine basis.

Follow this alignment procedure carefully because the setup of the video analogue path is critical to ensure the correct function of the Harry system.

(b) REQUIREMENTS

i. Colour monitor
ii. Waveform monitor
iii. Vectorscope
iv. Oscilloscope
v. Colour Bars 100%(PAL), 75% EIA (NTSC)
vi. Multiburst (monochrome for RGB)
vii. Pulse and Bar
viii. RGB Colour Bars

Note: The NTSC HARRY system is designed to accept video signals which have 7.5 IRE setup.

All front mounted Toggle switches should be in the up position with the exception of the RGB Input and Output option switches.

(c) SYSTEM WIRING

i. The Coded output should be connected directly to a colour monitor, a vectorscope and a waveform monitor.

ii. The Coded input should be fed directly from a signal generator with the appropriate test signal.

iii. When RGB inputs, other than RGB colour Bars, are required use a distribution amplifier.

iv. Ensure that the locking reference video signals are of the same horizontal and subcarrier phases as the test signal being used. This can be done by looping the video signal through the reference inputs and into the coded input

Note: All video connections required in these procedures should be made directly to the Harry unit.

3:4:2 **Output Timing card Alignment** (200374YA)

(a) Put the Output Timing card on an extender and use Colour bars as the output locking reference signal.

(b) Using the oscilloscope, monitor TP14 and adjust VC1 for maximum un-distorted demodulated chroma amplitude.

(c) Put the card back into the crate.

3:4:3 **Coder card Alignment** (17665C)

(a) Select Digital Colour Bars from the Engineering menu.

(b) Monitor the Coded output on the waveform monitor and adjust VR3 for a Luminance amplitude of 700mv (PAL), 714mv (NTSC) excluding syncs.

(c) Monitor the Coded output on the vectorscope and adjust VR2 for a vector amplitude of 100% (PAL), 75% (NTSC).

3:4:4 **RGB Output card Alignment** (17727C)

(a) Select Digital Colour Bars from the Engineering Menu.

(b) Monitor the GREEN output on the waveform monitor and adjust VR2 for a signal amplitude of 700mv (PAL), 714mv (NTSC) excluding syncs.

(c) Monitor the RED output on the waveform monitor and adjust VR1 for the correct RED Balance and signal amplitude of 700mv (PAL), 714mv (NTSC).

(d) Monitor the BLUE output on the waveform monitor and adjust VR4 for the correct BLUE Balance and signal amplitude of 700mv (PAL), 714mv (NTSC).

3:4:5 **Input Timing card Alignment** (200374YA)

(a) Put the Input Timing card on an extender board and use colour bars as the input/locking reference signal.

(b) Using an oscilloscope with correctly balanced probes, monitor TP14 and adjust VC1 for maximum un-distorted amplitude.

(c) Replace the card in the crate.

3:4:6 **ADC card Alignment** (17676D)

(a) Select Multiburst as the Coded input signal.

(b) Using the oscilloscope with correctly balanced probes, monitor TP11 and adjust VR7 to null out the LF Luminance frequencies of Multiburst. Adjust the delay line QD to reduce to a minimum the LF frequencies on TP11. Adjust the variable capacitor VC1 to minimize the LF frequencies.

(c) Select Live Coded input video, set the Menu Engineering Gain and Black level values to 128 and select Colour bars as the Main input signal. Set the system HUE/BURST PHASEs to the correct values.

Monitor the Main output, select Digital Multiburst, and adjust VR6 to provide the same picture black level when in and out of Adaptive filtering on the Chroma Proc card.

(d) Monitor the Coded output on the waveform monitor and adjust VR4/VR5 to make the black level/setup on the output 54mv (NTSC) 0 volts (PAL).

(e) Monitor the Coded output on the waveform monitor and adjust VR1/VR2 to make the Luminance amplitude on the output 714mv (NTSC) or 700mv (PAL). Re-adjustment of VR4/VR5 may be necessary.

(f) Monitor the Main output, select Multiburst as the Main input signal, and adjust VR3 to make the HF amplitude the same as the LF. The delay of QD may be slightly adjusted to minimize the LF/HF cross-over distortion, although this should not be necessary.

(g) Repeat as required to obtain the best performance.

3:4:7 **RGB Input Processor Alignment** (17723C)

(a) SYSTEM WITH CODED O/P CARD ONLY

Note: Make all adjustments to the nearest quiescent bit level.

i. Select RGB Colour Bars as the input to the system and monitor the Coded output on a vectorscope and waveform monitor.

Adjust VR3 for the correct Luminance gain on the Coded output.

Adjust VR1 to center the "V" axis vectors.

Adjust VR2 to center the "U" axis vectors.

iv. Repeat above until all are correct and check that the vector amplitudes are also correct.

v. Select Multiburst as the Red, Green and Blue input signals and check that the following is correct:

vi. Check that the frequency response of the Harry Coded output is flat within the specification.

(b) SYSTEM WITH RGB OUTPUT CARD

Note: Make all adjustments to the nearest quiescent bit level.

vii. Select RGB Colour Bars as the input to the system and monitor the Green output on a waveform monitor.

viii. Adjust VR3, very slightly, for the correct Green signal amplitude.

ix. Check that the Red output has the correct Luminance/Red balance. Adjust VR2 if necessary.

x. Check that the Blue output has the correct Luminance/Blue balance. Adjust VR1 if necessary.

xi. Repeat the above adjustments until the Red, Green and Blue outputs are correctly balanced.

xii. Select Multiburst as the Red, Green and Blue input signals and check that the following are correct:

Check that the frequency response of the Green output is flat within the specification.

xiii. Check that the frequency response of the Red output is flat within the specification.

xiv. Check that the frequency response of the Blue output is flat within the specification.

SECTION 5 : DIAGNOSTIC FACILITIES

3:5:1 Introduction

The Harry system contains various diagnostic aids both software and hardware which have been implemented to verify the correct operation of the system. The system's diagnostic facilities also allow faults to be quickly located.

All diagnostic facilities can easily be accessed from the front of the Harry unit using the PCB mounted toggle switches and from the user menu display using the Control system.

(a) HARDWARE FACILITIES

The hardware test facilities include; built-in digital test signals which allow the Decoder and Coder circuitry to be checked, built-in error detecting hardware which allows the video data path and store errors to be quickly isolated, and specific test facilities at card level to aid fault isolation.

(b) SOFTWARE FACILITIES

Software diagnostics fall into three main categories:

Computer self test.

Video and Disc hardware tests.

On-board test software.

3:5:2 Hardware Diagnostics Facilities

Note: For normal operation all red toggle switches MUST be in the up position. It is advisable to put all toggle switches UP (Normal position) to avoid confusion.

(a) ADC CARD (Coded Test Signals)

The switches on this card can be used to check the operation of the digital decoder. The Coded Test signals are selected by the rotary switch on the ADC card (17676) with switch SW1 in the down position. The Test signals available are selected by the position of the rotary switch:

SW2	TEST VIDEO
0-7	LIVE VIDEO
8-B	CODED COLOUR BARS (Not used)
C	MULTIBURST (part LF, part HF path)
D	MULTIBURST (all LF path)
E	RAMP (all HF path)
F	RAMP (all LF path)

(3,6A)

(b) CHROMA PROC CARD (Decode Test Signals)

There are various switches on this card which control the direction of the YUV paths through the card. These are mainly for checking the operation of the card itself. These switches can also be used to check the operation of the Disc path and Coder sections of the Harry system.

The lower toggle switch on the Chroma Proc card 17656A (PAL), 17654B (NTSC) can select a pseudo-random pattern identical on both Y and U/V data paths:

UP	NORMAL VIDEO
MIDDLE	COPY Y TO U/V
DOWN	PSEUDO RANDOM PATTERN

There is also a switch provided which forces the adaptive decoder into either "Comb" or "Simple" which can be used for video inputs that are difficult to decode.

Decoded Test video is also produced by the system computer, which can write Colour Bars Multiburst and Ramp into store section of the system.

(c) STORE CONTROL CARD

When the lower toggle switch on this card is in the down position the Store Control card is forced to read from a single "stripe" of the I/O Store. The Stripe (0-12) is selected by the rotary switch SW2. Note: the number on this switch is not the stripe number:

SWITCH 2	STRIPE
4	11
5	10
6	9
7	8
8	7
9	6
A	5
B	4
C	3
D	2
E	1
F	0

When the upper toggle switch is in the down position the "Reel RAMs" are bypassed. This can be used if trouble is experienced with the Reels, to locate possible errors.

(d) INPUT SWITCH CARD

When the toggle switch on this card is in the down position the Luminance and Chrominance are swapped. It is usually easier to find a Chrominance satellite fault when Luminance grey wedge signal is used rather than a signal like Colour bars.

With this switch down, the lower satellites will be used to store and process Luminance. Unfortunately this also swaps Y and U/V in the menu, making it difficult to read. It can, however, be changed just at the appropriate moment.

(e) MUX/DEMUX CARD

With the top switch in the down position Test mode is enabled.

In test mode when the second toggle switch is in the UP position only the left satellite is enabled when reading. In the centre position, both satellites are turned off when reading and a grey level/zero chrominance is substituted. In the down position, only the right hand satellite is enabled when reading. Note: that in these modes pixels are being duplicated and that all satellites still record, regardless of the position of these switches.

The DIL switch on this card provides the facility to force individual data bits when Reading from the satellites. This allows missing or stuck bits to be found. Two sockets are provided (active only on the upper Mux/Demux) to enable comparisons between satellites. The output is wired to the TEST BNC socket on the rear panel. The toggle switch just above the ex-ored sockets selects either satellite read or write clocks to clock the result of the ex-or operation.

The Test Probes allow identical data points to be checked. This can be used to quickly locate errors to component level. The probes can be used to find faults on any cards where there are parallel data paths that can be made identical.

Differences found between the test probes are displayed using the Test output connected to a standard monochrome monitor. Errors are displayed on the monitor as white on black.

Caution: Do not let the Test Probes touch the +&- 12 volt power rails as this will destroy the checking circuitry on the Mux/Demux card.

(f) STORE ADDRESS CARD

The toggle switch on this card forces the Store Control to read from only a single stripe in the Satellite Store. The Stripe (1-4) is selected by the rotary switch just below it. Note: The number on the switch is not the stripe number:

SWITCH 2	STRIPE
0,4,8,C	4
1,5,9,D	3
2,6,A,E	2
3,7,B,F	1

(g) DISC CONTROLLER CARD

When the toggle switch on this card is in the down position, the Open Cable line to the Disc is opened. The disc will therefore ignore all commands from the Harry mainframe. The three numeric displays show the line in the micro program which the Disc Controller is executing. The displays on all four satellites should be exactly the same, indicating that if one is different then there is a problem.

(h) DISC INTERFACE CARD

When the red LED on the front of this card is illuminated, the Disc is not in rotation sync. This usually indicates that either a cable has been removed or the Disc switches have been changed from their normal positions.

(i) RGB INPUT CARD

This card has test signal switches which allow RGB Test signals to be substituted for the RGB input video.

(j) CPU CARD

This card holds a simple software monitor program, which on power up performs self tests to check the function of the CPU card. This monitor can be accessed via the 10-way RS 232 port on the front of the CPU card.

(3,6A)

3:5:3 Software Test Facilities

(a) COMPUTER SELF TEST

On system power up or reset the Harry system computer runs through system check then displays the user menu. This checks the integrity of the Micro Code Programs held in RAM on the Disc Controller cards and the RAM on the Combiner cards. This process also checks the system computer bus and the Disc Controller circuitry.

(b) VIDEO AND DISC HARDWARE TESTS

To enter the software diagnostics, select MISC, then DIAGNOSTICS and the following menu of options will be displayed:

END DIAG
I/O STORE TESTS
SAT STORE TESTS
DISC TESTS
COMBINER TESTS
MISC TESTS

(c) END DIAG

When this is selected the display returns to the user menu.

(d) I/O STORE TESTS

When this is selected a new sub-menu is displayed to the right. This allows signals to be written into the I/O Store; Video, digital input signals or a test pattern (grey wedge or colour bars). If the "continuous" box is not selected (white) the write will cease after one frame. If the "continuous" box is selected (pink) the write is continuous.

The "roll reels" box has a number box next to it. This selects which reel format is to be used. There is a prom on the I/O Store Control driven by the read horizontal counters with eight different formats programmed into it.

The "chequer" command will roll the reels with a check pattern, thus defining the boundaries between the reels.

(e) SAT STORE TESTS

Note: The Satellite stores can only be written or read, not both at the same time.

When this is selected a new sub-menu is displayed to the right. This is similar to the I/O Store sub-menu with separate read and write boxes and six selectable boxes (1-6). These select which satellite store(s) that are to be read or written. The "continuous" box will make the Read or Write operation continuous. Tapping the pen down will stop the function at the end of a cycle (note you may have to wait a few seconds).

(3,6A)

Write Buffer: Either a test pattern (Colour bars or grey wedge) or live video may be written into one or all of the satellite stores. The stores 1-6 which are selected (pink box) will be written. Note that stores 1-3 are the left hand Buffer Stores and 4-6 are the right hand cards.

Read Buffer: Any of the six satellite stores may be read, continuously if set, by selecting "Read Buffer" then the number.

Get Colour: (Normally used in continuous mode). Select Get Colour then the store number, and the cursor should now be the colour of the picture underneath it. Tap the pen down to stop.

(f) DISC TESTS

Write disc and Read disc access a normally-unused track on the disc. The contents of one of the satellite stores may be transferred to and from this track, thus exercising the discs and the data paths to and from them.

Reset discs: Reloads the micro code into the disc controllers and sends a Fault Clear command to the discs, getting them back to the Start-up condition.

Seek: Cycles the disc through all the cylinders; the diagnostic lights inside each disc front panel should count from zero to 840, if the DIAG switch is set to CAR. Note all Discs should be identical.

Check read and Check write are not yet implemented

(g) COMBINER TESTS

Not yet implemented.

(h) DISC TESTS

Addr and Data allow any register on the system bus to be Loaded with known data values. These registers may be written continuously if necessary.

Note: When in Continuous the current timecode being read is displayed.

SECTION 6 : DIAGNOSTICS QUICK REFERENCE GUIDE(3,6B)

3:6:1 Introduction

This section contains details of the front mounted switches and diagnostics facilities.

3:6:1 Introduction 95
3:6:2 17600 CIO Card 97
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(3,6B)

Bottom Rack Highway

BE01	Disk Controller	17711
BE02	Disk Interface	17713
BE03	Data Select	17730
BE04	Combiner	17732
BE05	Buffer Store 1	17715
BE06	Buffer Store 2	17715
BE07	Store Address	17716
BE08	Disk Controller	17711
BE09	Disk Interface	17713
BE10	Data Select	17730
BE11	Combiner	17732
BE12	Buffer Store 1	17715
BE13	Buffer Store 2	17715
BE14	Store Address	17716
BE15	Mux/Demux	17717
BE16	Audio Proc	2003716
BE17		
BE18		
BE19	I/P Timing	200374Y
BE20	Chroma Filter	17673
BE21	Chroma Proc	17654
BE22	ADC	17676
BE23	RGB Input	17727
BE24	O/P Timing	200374Y
BE25	Coder	17655
BE26	RGB Output	17723

Top Rack Highway

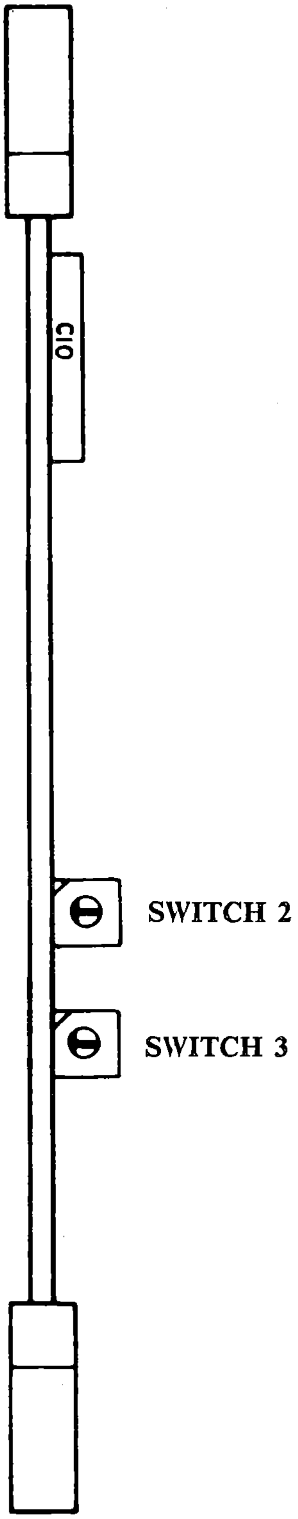
TE01	Disk Controller	17711
TE02	Disk Interface	17713
TE03	Data Select	17730
TE04	Combiner	17732
TE05	Buffer Store 1	17715
TE06	Buffer Store 2	17715
TE07	Store Address	17716
TE08	Disk Controller	17711
TE09	Disk Interface	17713
TE10	Data Select	17730
TE11	Combiner	17732
TE12	Buffer Store 1	17715
TE13	Buffer Store 2	17715
TE14	Store Address	17716
TE15	Mux/Demux	17717
TE16		
TE17		
TE18	Input Switch	17718
TE19	I/O Store	17710
TE20	I/O Store	17710
TE21	I/O Store Control	17720
TE22	Codec	2003732
TE23	Time Code	17724
TE24		
TE25	CPU	17601
TE26	CIO	17600
TE27	ROM/RAM	17728

Note that the 17654 card is replaced by 17656 in the PAL system and 17673 is replaced by 17657 card.

Note: E01 is the first left hand card slot in the rack.

3:6:2 17600 CIO Card

Figure 3.6.1



The rotary switches on the CIO card should be set to 0-NTSC or 8-PAL (bottom switch) and 0 (top switch).

The system software can operate in a number of control modes, designated by the rotary switches on this card. To obtain these control modes, it is necessary to set the rotary switches on the CIO card to the appropriate positions and to reset the system. The two switches form an 8-bit word, whose bits are designated as follows:

Bit	**Operation**
0	Not used
	0 = NTSC Operation
1	1 = Ignore but Report Hardware errors
2	Not Used
3	1 = Full Speed Combiner operation
4	1 = Development Software enabled
5	Not Used
6	Not Used
7	1 = PAL Operation

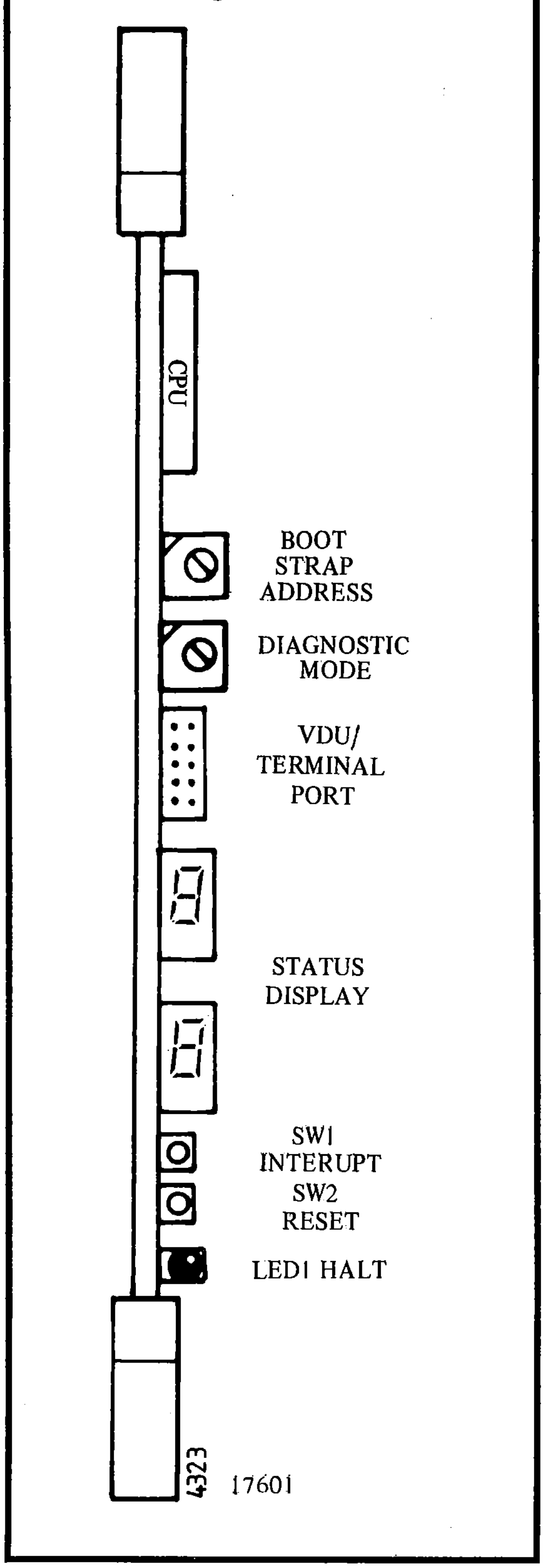
The following table gives information on the various settings:

SWITCH 2	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Bit 0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Bit 1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
Bit 2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
Bit 3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

SWITCH 3	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Bit 4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Bit 5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
Bit 6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
Bit 7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

3:6:3 17601 CPU Card

Figure 3.6.2



The rotary switches on the CPU card should be set to F (top switch) and 0 (bottom switch). These switches determine the source of the system operating software (F : RAM/ROM card).

Note: Positions 0 to E on the CPU card top switch are not used.

SWITCH 3 BOOT STRAP ADDRESS

This switch determines which software is to be booted from the system RAM/ROM card. (See Chapter 2 section 8 and Chapter 3 section 5 for details)

VDU/TERMINAL PORT

This gives access to the system computer for Test/Servicing purposes and to access the CPU Monitor program.

STATUS DISPLAY

This indicates the status of the system computer when software is booting and while the system is running.

SWITCH 1

This switch is used to interrupt the system computer. Switch 1 can be used for diagnostic purposes in conjunction with the VDU port. Note that after switch 1 is pressed the system must be reset.

SWITCH 2

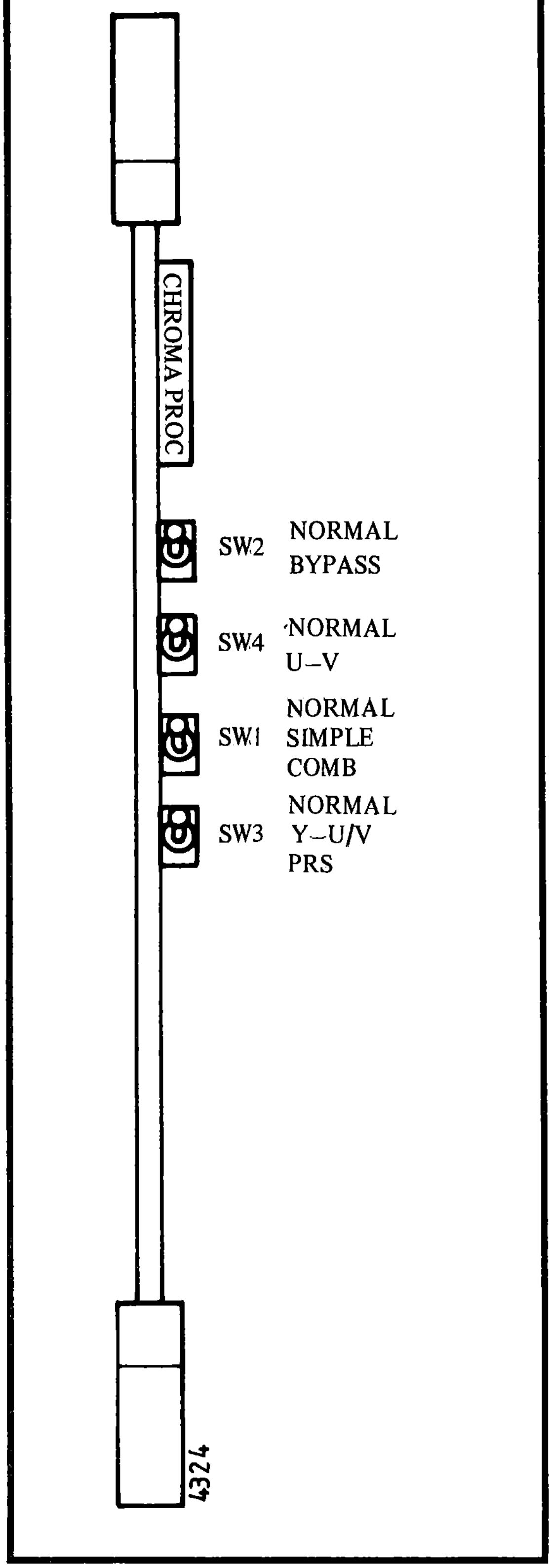
This switch is used to reset the system computer and Boot the system. (See Chapter 2 section 8 for details)

LED 1

When on this LED indicates that the system computer has been halted.

3:6:4 17654 Chroma Processor Card (NTSC)

Figure 3.6.3



There are various switches on this card which switch the YUV paths through the card. These are mainly used for checking the operation of the card itself, but, can be used to check the operation of the Disk path and Coder sections of the system.

SWITCH 2

This switch bypasses the "U" demodulator circuit, so that monochrome Test signals can be passed through the card unmodulated.

SWITCH 4

This switch copies the "U" data onto the "V" data path, at the output of the "U" demodulator circuit, so that monochrome Test signals can be passed identically down the "U" and "V" data paths.

SWITCH 1

This switch determines the filtering process used by the Chroma Proc:

Normal: Adaptive Comb Filtering
Simple : Not Combed
Comb : Comb filtering only

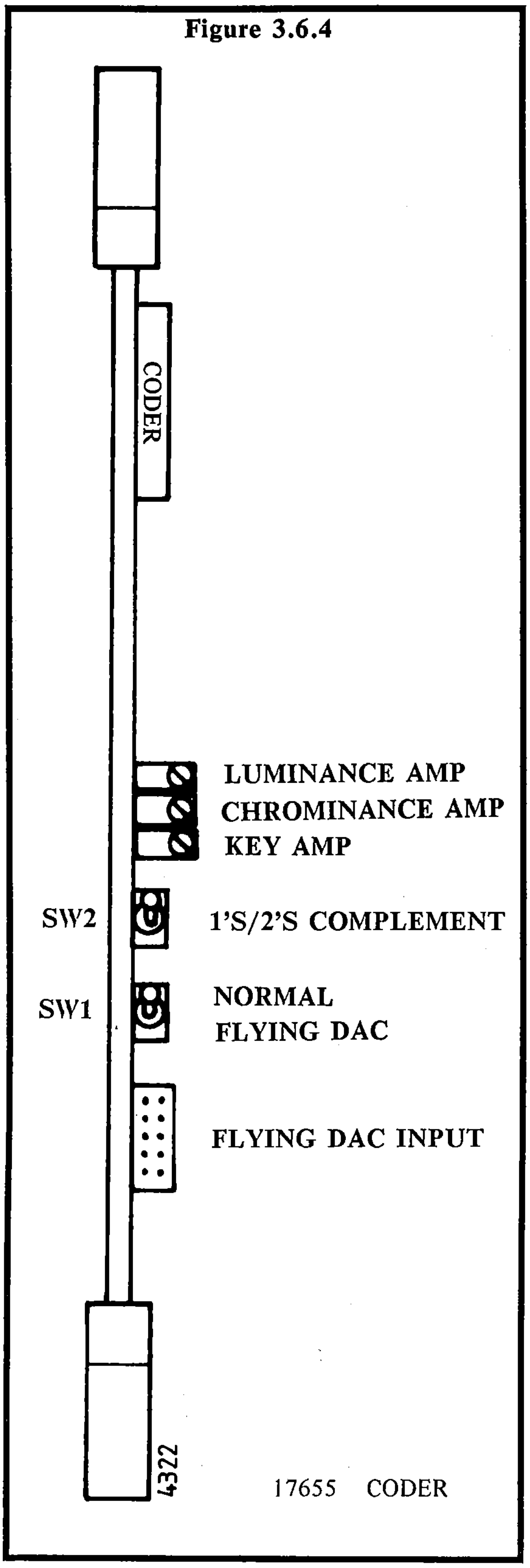
SWITCH 3

Y-U/V: Y data is copied onto the U/V data path.

PRS : Random Test signal on Y and U/V data paths

3:6:5 17655 Coder Card

Figure 3.6.4



VR3 LUMINANCE AMP

This is the preset adjustment for the Wide band Luminance and sync pulse output signal amplitude.

VR2 CHROMINANCE AMP

This is the preset adjustment for the Chrominance and Burst output signal amplitude.

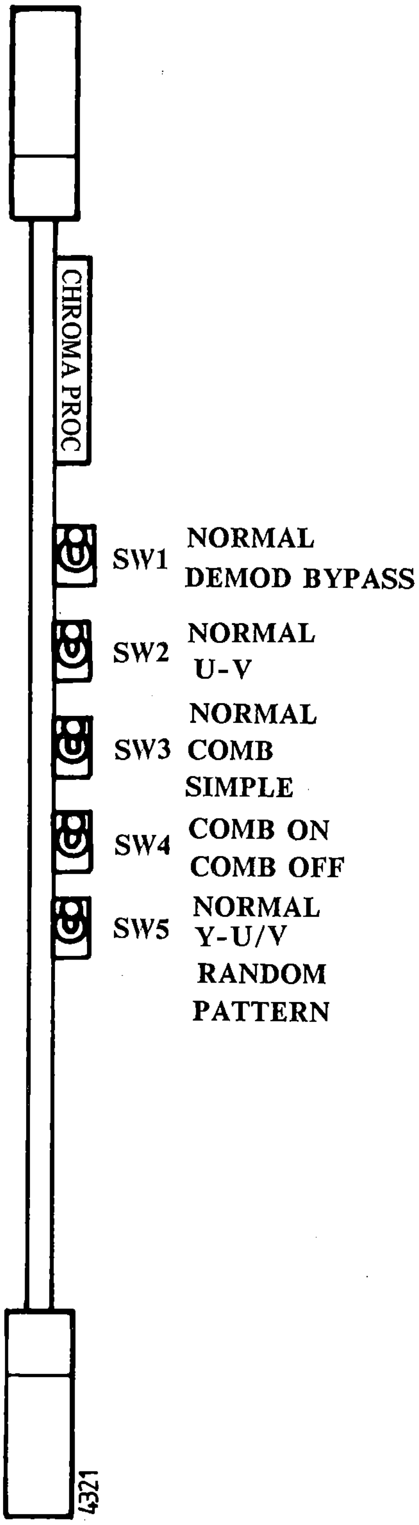
VR1 AMP (not used)

SWITCH 2 (not used)

SWITCH 1 (not used)

3:6:6 17656 Chroma Processor card (PAL)

Figure 3.6.5



There are various switches on this card which switch the YUV paths through the card. These are mainly used for checking the operation of the card itself, but, can be used to check the operation of the Disk path and Coder sections of the system.

SWITCH 1

This switch bypasses the "U" demodulator circuit, so that monochrome Test signals can be passed through the card unmodulated.

SWITCH 2

This switch copies the "U" data onto the "V" data path, at the output of the "U" demodulator circuit, so that monochrome Test signals can be passed identically down the "U" and "V" data paths.

SWITCH 3

This switch determines the filtering process used by the Chroma Proc:

NORMAL	: Adaptive Comb Filtering
COMB	: Comb filtering only
SIMPLE	: Not Combed

SWITCH 4

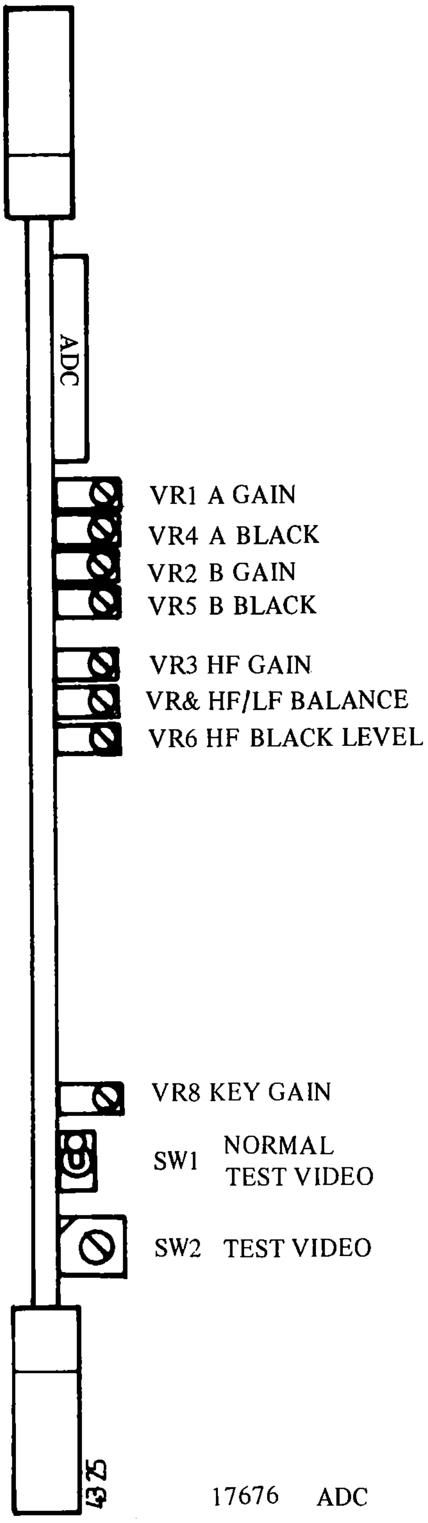
This switch turns off the Post demodulator Comb circuits, to produce simple filtering.

SWITCH 5

Y-U/V: In this position the Y data is copied onto the U/V data path.
PRS: In this position, a randomly changing Test signal is put onto the Y and U/V data paths

3:6:7 17676 ADC Card

Figure 3.6.6



The switches on this card can be used to check the operation of the digital decoder. The Coded Test signals are selected by the rotary switch on the ADC card (17676) with switch SW1 in the down position.

VR1 VIDEO GAIN

This is the wide band Coded input video Gain preset adjustment

VR2 VIDEO GAIN

(Not used)

VR3 HF + CHR GAIN

This is the HF + CHR Gain preset adjustment

VR4 CODED INPUT BLACK LEVEL

This is the Coded input Black Level preset adjustment

VR5 B INPUT BLACK LEVEL

(Not used)

VR6 HF + CHR ADC OFFSET

This is the HF ADC offset preset adjustment

VR7 HF/LF SUBTRACTER BALANCE

This is the common HF/LF subtracter balance preset adjustment

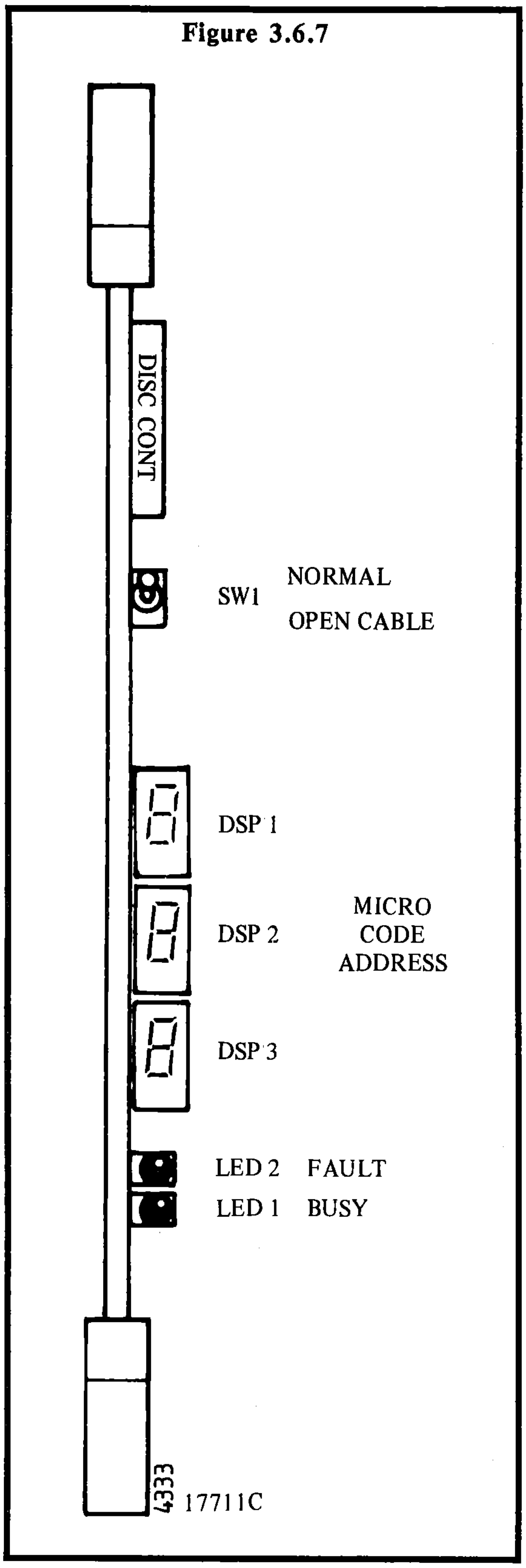
SWITCH 1

When in the down position, this switch enables the Test videos selected by switch 2:

0-3 : Encoded Colour Bars
4 : LF and HF Multiburst
5 : LF Multiburst
6 : LF Ramp
7 : HF Ramp

3:6:8 17711 Disk Controller Card

Figure 3.6.7



When the toggle switch on this card is in the down position, the "Open Cable line" to the Disk is opened. The Disk will therefore ignore all commands from the Harry system.

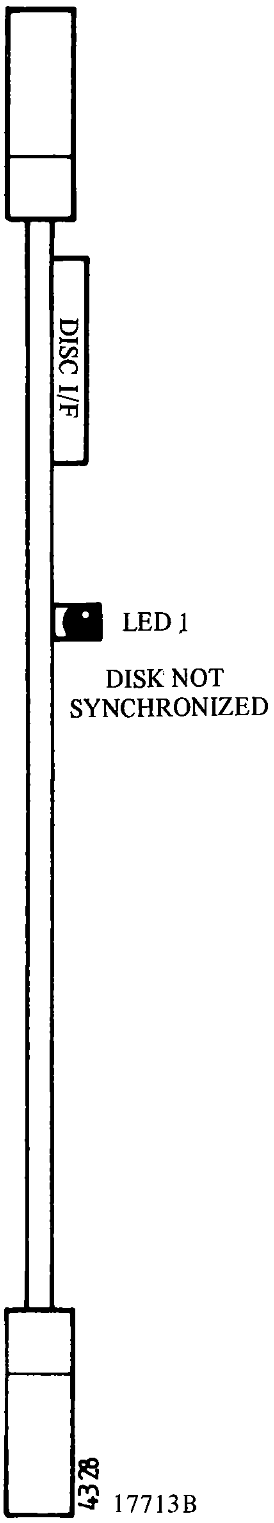
The three numeric displays show the line in the micro program which the Disk Controller is executing. The displays on all four satellites should be exactly the same, indicating that if one is different then there is a problem.

LED 2 shows a fault condition with either the card or the Disk Drive. This may be cleared by *RESET DISK* within the *DISK TESTS* menu under *MISC & DIAGNOSTICS.*

LED 1 shows that the Disk Controller card is accessing the Disk Drive.

3:6:9 17713 Disk Interface Card

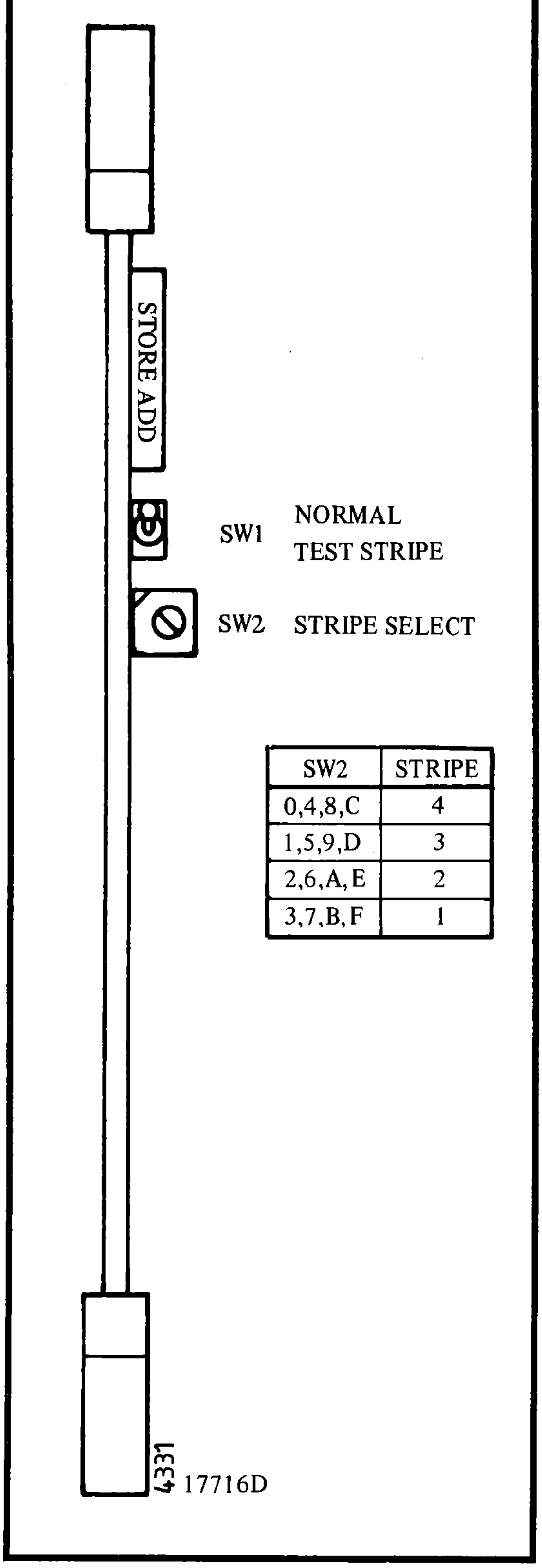
Figure 3.6.8



When the red LED on the front of this card is illuminated, the Disk is not in rotation sync. This usually indicates that either a cable has been removed or the Disk switches have been changed from their normal positions.

3:6:10 17716 Store Address Card

Figure 3.6.9

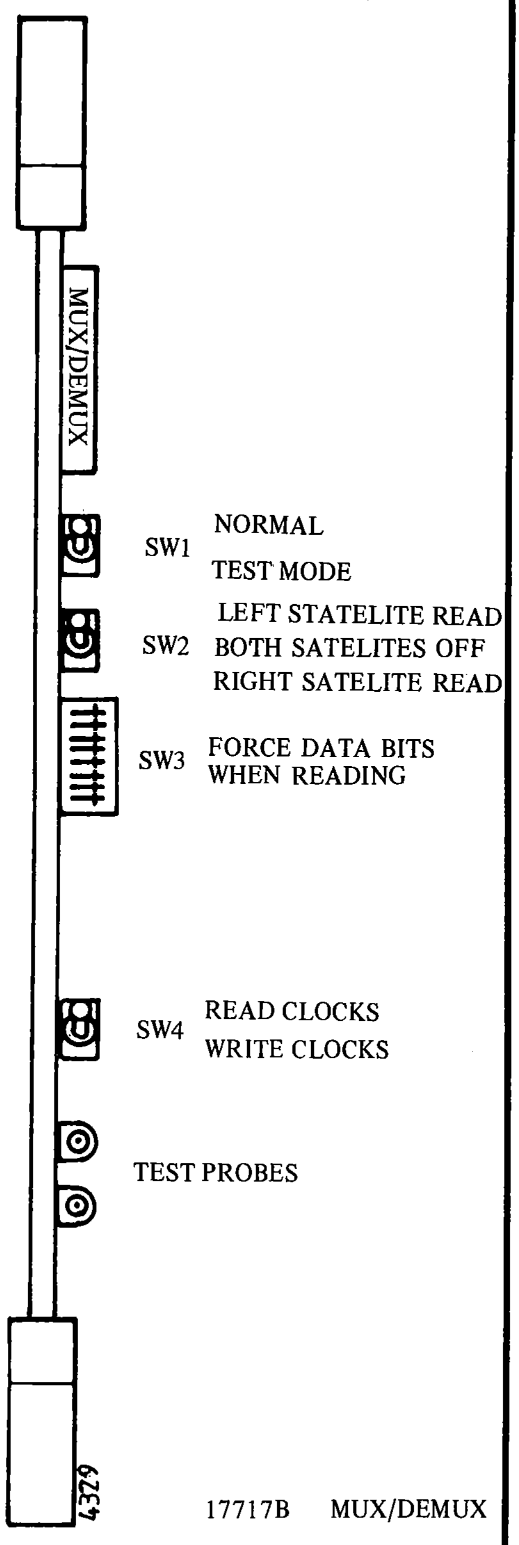


SW2	STRIPE
0,4,8,C	4
1,5,9,D	3
2,6,A,E	2
3,7,B,F	1

The toggle switch on this card forces the Store Control to read from only a single stripe in the store. The Stripe (1-4) is selected by the rotary switch just below it. Note: The number on the switch is not the stripe number:

3:6:11 17717 Mux/Demux Card

Figure 3.6.10



With the top switch in the down position the card Test mode is enabled.

In test mode, when the second toggle switch is in the UP position, only the left satellite is enabled when reading. In the centre position, both satellites are turned off when reading and a grey level/zero chrominance is substituted. In the down position, only the right hand satellite is enabled when reading. Note: that in these modes pixels are being duplicated and that all satellites still record, regardless of the position of these switches.

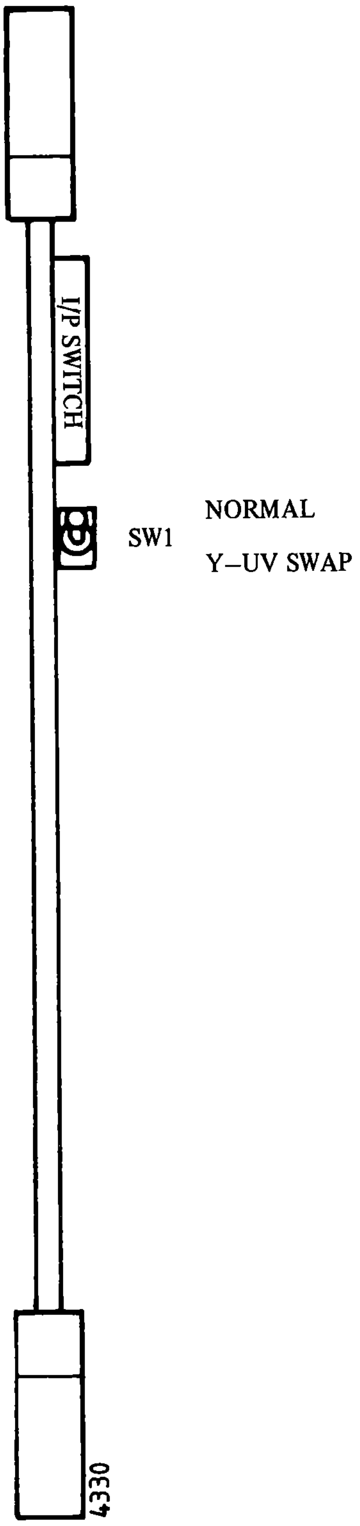
The DIL switch on this card provides the facility to force individual data bits when Reading from the satellites. This allows missing or stuck bits to be found. Two sockets are provided (active only on the upper Mux/Demux) to enable comparisons between satellites. The output is wired to the TEST BNC socket on the rear panel. The toggle switch just above the ex-ored sockets selects either satellite read or write clocks to clock the result of the ex-or operation.

The Test Probes allow identical data points to be checked. This can be used to quickly locate errors to component level. The probes can be used to find faults on any cards where there are parallel data paths that can be made identical.

Differences found between the test probes are displayed using the Test output connected to a standard monochrome monitor. Errors (differences between the probes) are displayed on the monitor as white on black.

3:6:12 17718 Input Switch Card

Figure 3.6.11

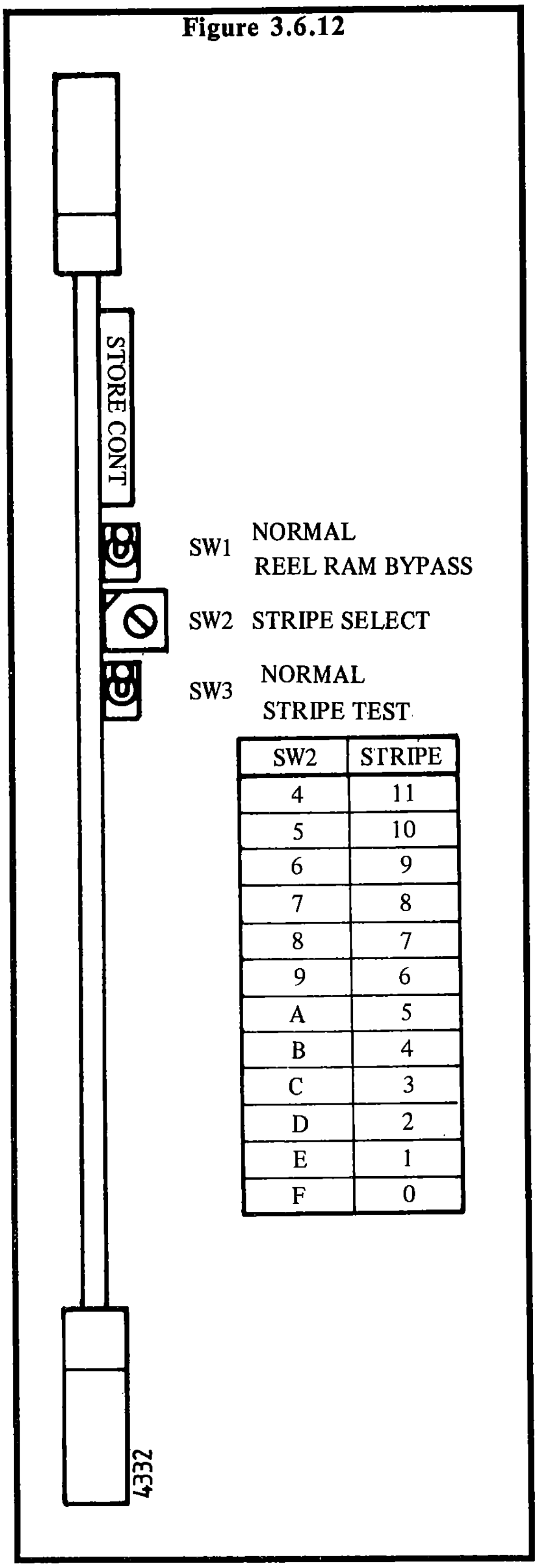


When the toggle switch on this card is in the down position the luminance and chrominance data are swapped. It is usually easier to find a chrominance satellite fault when luminance grey wedge signal is used rather than a signal like Colour bars.

With switch 1 down, the lower satellites will be used to store and process luminance. Unfortunately this also swaps Y and U/V in the menu, making it difficult to read. It can, however, be changed just at the appropriate moment.

3:6:13 17720 I/O Store Control Card

Figure 3.6.12



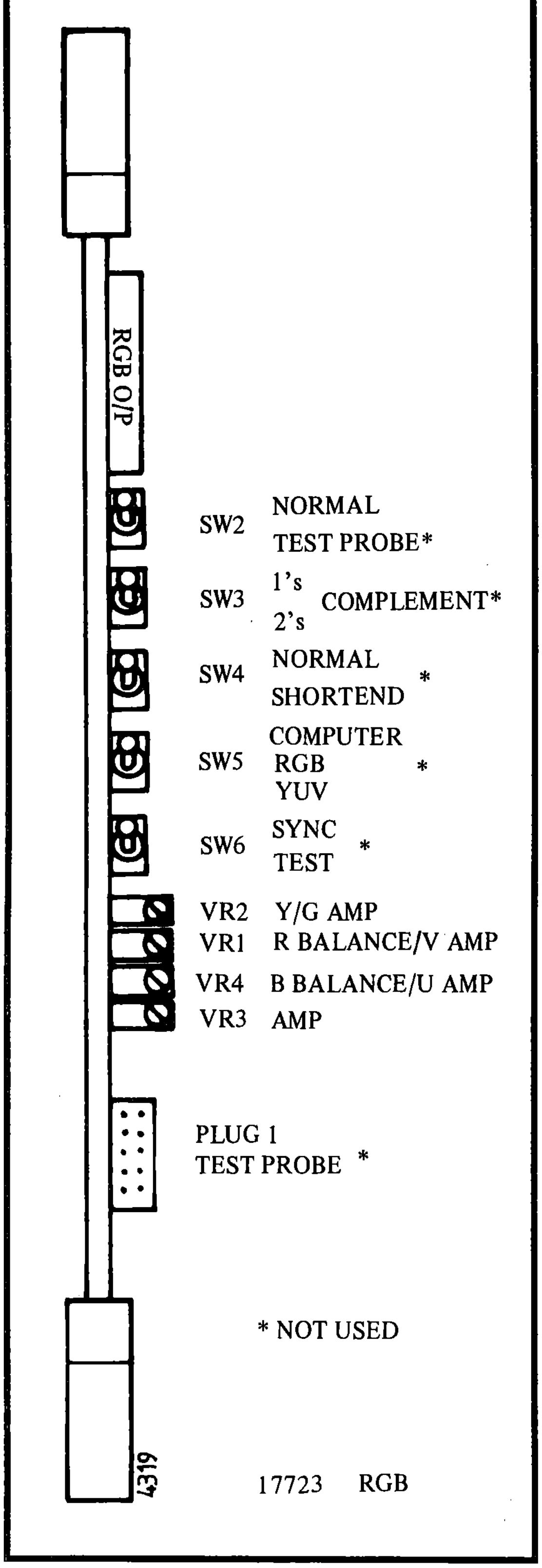
SW2	STRIPE
4	11
5	10
6	9
7	8
8	7
9	6
A	5
B	4
C	3
D	2
E	1
F	0

When the lower toggle switch on this card is in the down position the Store Control card is forced to read from a single "stripe" of the I/O Store. The Stripe (0-12) is selected by the rotary switch just above it. Note: the number on the switch is not the stripe number:

When the upper toggle switch is in the down position the "Reel RAMs" are bypassed. This can be used to isolate the Reel RAMs.

3:6:14 17723 RGB Output Card

Figure 3.6.13



This card gives either RGB or YUV outputs determined by switch 1 and the links on the RGB output card:

SW2 (not used)

SW3 (not used)

SW4 SHORTEN (not used)

SW5 RGB/YUV

This switch, in conjunction with links on this card, is used to select RGB or YUV output operation.

UP	COMPUTER
MIDDLE	RGB OUTPUT
DOWN	YUV OUTPUT

SW6 SYNC/TEST

This switch is used to select output syncs or the Test output.

VR2

This is the Luminance/Green output amplitude preset adjustment.

VR1

This is the (Red balance)/(V amplitude) preset adjustment.

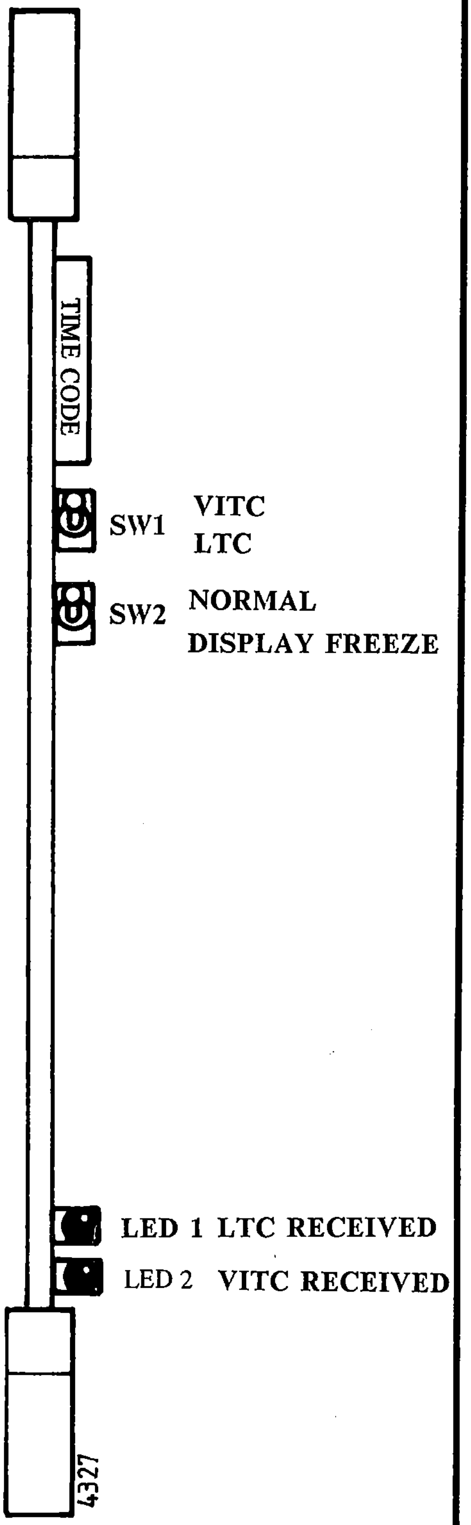
VR4

This is the (Blue balance)/(U amplitude) preset adjustment.

VR3 (not used)

3:6:15 17724 Time Code Card

Figure 3.6.14



SWITCH 1

This switch is used to select either the VITC or LTC Time code information.

SWITCH 2

This switch, when in the down position is used to freeze the Time code information displayed.

LED 1

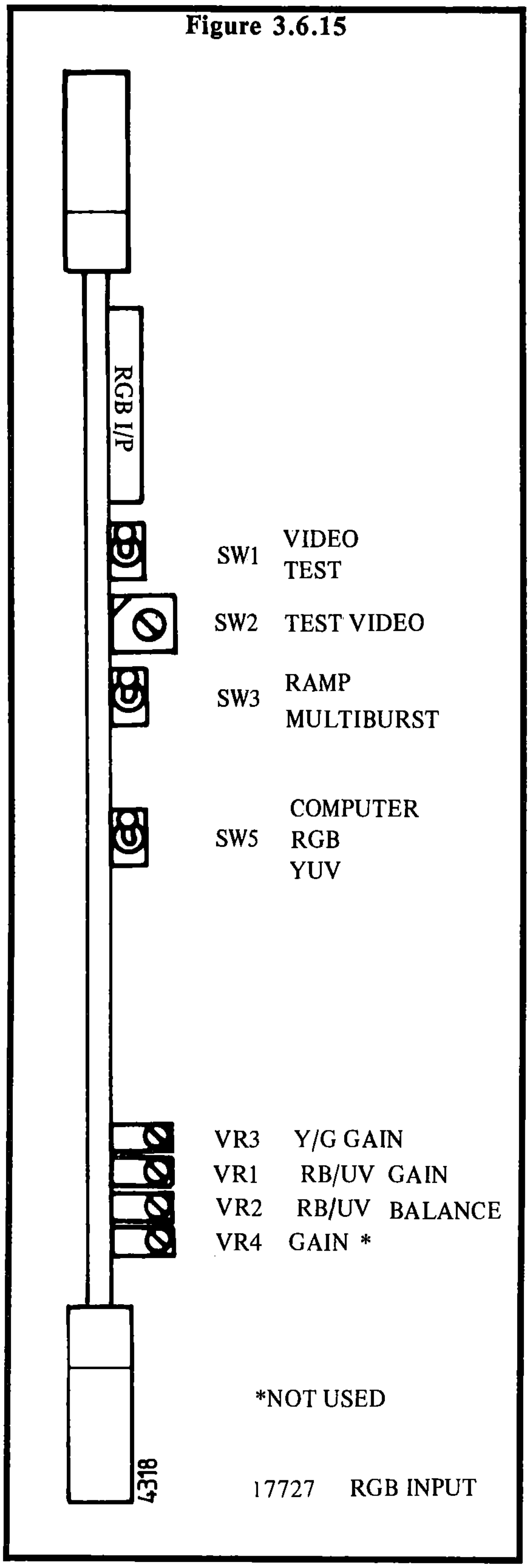
This LED displays whether the LTC Time code information has been received correctly.

LED 2

This LED displays whether a VITC Time code has been received.

3:6:16 17727 RGB Input Card

Figure 3.6.15



SW1 VIDEO/TEST

This switch when in the down position enables the test video selected by switch 2 and switch 3

SW2 TEST VIDEO

This rotary switch selects various test videos:

0,8	RGB Ramp
1,9	Green Ramp
2,A	Blue Ramp
3,B	Blue/Green Ramp
4,C	1/2 amplitude RGB Ramp
5,D	1/2 amplitude Green Ramp
6,E	1/2 amplitude Blue Ramp
7,F	Black

SW 3 RAMP/MULTIBURST

This switch selects between digitally generated Ramp and digitally generated Multiburst test videos.

SW5 RGB/YUV

This switch in conjunction with links on this card determines whether the card accepts RGB or YUV input video signals.

UP	COMPUTER
MIDDLE	RGB INPUT
DOWN	YUV INPUT

VR3

This is the preset adjustment for GREEN or Y Gain.

VR1

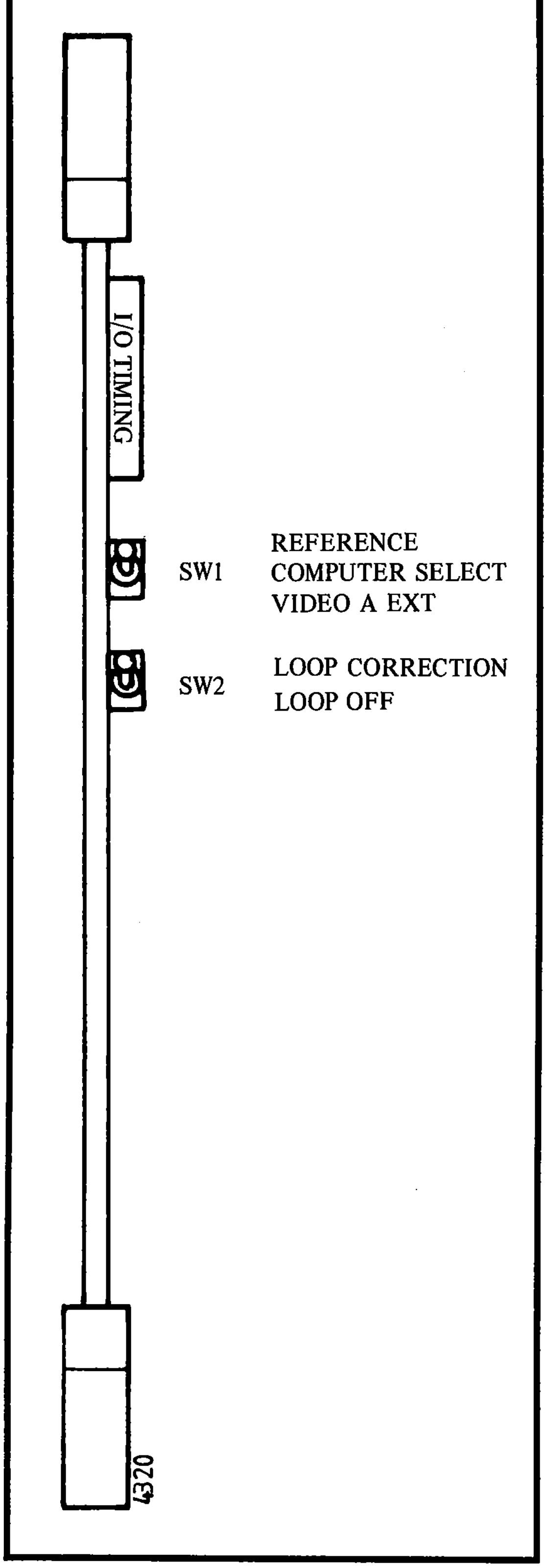
This is the preset adjustment for RED/BLUE Gain or U/V Gain.

VR2

This is the preset adjustment for RED/BLUE balance or U/V balance.

3:6:17 200374Y I/O Timing Card

Figure 3.6.16



SWITCH 1

This switch is only used on the Input Timing card, to select between Coded input and Input Reference sources of locking video; UP-Input Reference video, Middle-computer selectable, and Down-Coded input.

SWITCH 2

When in the down position, this switch turns off the phase correction of the burst locked subcarrier generator. This produces a line locked subcarrier, which is not phase locked to the reference burst.

SECTION 7 : CABLE AND SOCKET DETAILS

3:7:1 Video Signal Connections

(a) VIDEO INPUTS

Socket	**Printed Circuit Board** **Board**	 **Slot**	 **Pin**
VID	ADC CARD	BE 22	A11
Green	RGB I/P	BE 23	A11
Red	RGB I/P	BE 23	A16
Blue	RGB I/P	BE 23	B18
Sync	I/P TIMING	BE 19	A12
Input Vid Ref	I/P TIMING	BE 19	A14
Output Vid Ref	O/P TIMING	BE 24	A14

(b) VIDEO OUTPUTS

Socket	**Printed Circuit Board** **Board**	 **Slot**	 **Pin**
Vid Main	CODER	BE 25	A12
Vid Aux	CODER	BE 25	A18
Green	RGB O/P	BE 26	A12
Red	RGB O/P	BE 26	A18
Blue	RGB O/P	BE 26	A16
Sync	RGB O/P	BE 26	A38
Test	Mux/Demux	TE 15	A69

3:7:2 Control Signal Input Connections

(a) TIME CODE INPUT

This is a 3-pin XLR connector which is used to input an EBU Standard Longitudinal Time Code signal to the Harry system. The Time Code input is a balanced pair, which also can be used un-balanced by taking either pin to ground. The amplitude of the analogue Time code signal should be stable within the amplitude range of 0.55 volts pk-pk to 10 volts pk-pk into an input impedance of approximately 10,000 ohms

Note the polarity of the balanced pair is not critical.

XLR Pin	Function	Printed Circuit Board Board	Slot	Pin
1	Time Code	Time Code	TE 23	A15
2	Time Code	Time Code	TE 23	B15
3	Screen	Time Code	TE 23	

(b) VDU/TERMINAL SOCKET (CPU card)

This socket gives access to the system computer so that software diagnostics can be accessed.

pin	2	0 volts
pin	3	output to terminal
pin	8	input from terminal

RS 232 9600 baud.

(c) PAINTBOX

This is a 9-way D-type socket which provides the RS 422 data link to the Paintbox.

PAINTBOX Pin	Function	Printed Circuit Board Board	Slot	Pin
1	0 Volts	CODEC	TE 22	
2	Receive Data -	CODEC	TE 22	A61
3	Transmit Data +	CODEC	TE 22	B62
7	Receive Data +	CODEC	TE 22	B61
8	Transmit Data -	CODEC	TE 22	A62

(d) TABLET

This is a 9-way D-type socket which provides the RS 422 data link to the Tablet.

TABLET Pin	**Function**	**Printed Circuit Board** **Board**	**Slot**	**Pin**
1	0 Volts	CODEC	TE 22	
2	Receive Data -	CODEC	TE 22	A38
3	Transmit Data +	CODEC	TE 22	B40
7	Receive Data +	CODEC	TE 22	B38
8	Transmit Data -	CODEC	TE 22	A40

(e) AUDIO IN

This is a 3-pin XLR connector which is used to input an audio signal to the system. This signal is used by the system to provide a low bandwidth scratch track. The audio input accepts a wide input signal amplitude range into a selectable input impedance of 150 Ohms, 200 Ohms, 620 Ohms or 50 KOhms.

XLR Pin	**Function**	**Printed Circuit Board** **Board**	**Slot**	**Pin**
1	Audio input	Audio Proc	BE 16	A11
2	Audio input	Audio Proc	BE 16	B11
3	Screen			

(f) AUDIO OUT

This is a 3-pin XLR connector which is used to output the system's audio scratch track.

XLR Pin	**Function**	**Printed Circuit Board** **Board**	**Slot**	**Pin**
1	Audio Output	Audio Proc	BE 16	A14
2	Audio Output	Audio Proc	BE 16	B14
3	Screen			

(e) COMMS (not yet implemented)

This is a 9-way D-type socket providing an RS 422 connection to an external device.

COMMS Pin	**Function**	**Printed Circuit Board** **Board**	**Slot**	**Pin**
1	0 Volts	CIO CARD	TE 27	
2	Receive Data -	CIO CARD	TE 27	A55
3	Transmit Data +	CIO CARD	TE 27	B56
7	Receive Data +	CIO CARD	TE 27	B55
8	Transmit Data -	CIO CARD	TE 27	A56

(f) PRINTER (not yet implemented)

This is a 9-way D-type socket providing an RS 232 connection to an external device.

PRINTER Pin	**Function**	**Printed Circuit Board** **Board**	**Slot**	**Pin**
1	0 Volts	CIO CARD	TE 27	
2	Receive Data	CIO CARD	TE 27	A52
3	Transmit Data	CIO CARD	TE 27	B52

(g) TEST/PAINTBOX REMOTE

This is a 9-way D-type socket providing an RS 422 connection to the Paintbox.

TEST Pin	**Function**	**Printed Circuit Board** **Board**	**Slot**	**Pin**
1	0 Volts	CIO CARD	TE 27	
2	Receive Data	CIO CARD	TE 27	A53
3	Transmit Data	CIO CARD	TE 27	B54
7	Receive Data +	CIO CARD	TE 27	B53
8	Transmit Data -	CIO CARD	TE 27	A54

(h) REMOTE

This 37-way connector provides the input and output cue lines when the Time code card is fitted. The Remote socket pins are designated as follows:

REMOTE Pins	Function	Printed Circuit Board Board	Slot	Pins
8, 27	Output Cue 1	Time Code	TE 23	A40,B40
7, 26	Output Cue 2	Time Code	TE 23	A41,B41
6, 25	Output Cue 3	Time Code	TE 23	A42,B42
5, 24	Output Cue 4	Time Code	TE 23	A43,B43
4, 23	Output Cue 5	Time Code	TE 23	A44,B44
3, 22	Output Cue 6	Time Code	TE 23	A45,B45
2, 21	Output Cue 7	Time Code	TE 23	A46,B46
1, 20	Output Cue 8	Time Code	TE 23	A47,B47
9, 28	Output Cue 9	Time Code	TE 23	A48,B48
11,30	Output Cue 10	Time Code	TE 23	A50,B50
12,31	Output Cue 11	Time Code	TE 23	A51,B51
13,32	Output Cue 12	Time Code	TE 23	A52,B52
36,37	Over-temp Alarm			
17	Input Cue 1	Time Code	TE 23	A56
16	Input Cue 2	Time Code	TE 23	A55
15	Input Cue 3	Time Code	TE 23	A54
14	Input Cue 4	Time Code	TE 23	A53
18,19	+ 5 volts	Time Code	TE 23	A57,A58
29,33	0 volts	Time Code	TE 23	B59-B53
34,35	0 volts	Time Code	TE 23	
10	No connection	Time Code	TE 23	A49

3:7:3 Data Connections

(a) INPUT CHANNELS 1-4

The two 25-way D-Type connectors (Channel 1 and 2) provide EBU 601 standard digital video inputs. The two 50-way ribbon connectors (Channel 3 and 4) provide Quantel standard digital video inputs. These 4 inputs are routed through the I/O Expander Input card to the Chroma Processor card.

QUANTEL I/F Pin	Function	Printed Circuit Board Board Slot	Pin
1	Y IN 0H	Chroma Proc BE 21	B37
3	Y IN 1H	Chroma Proc BE 21	A38
5	Y IN 2H	Chroma Proc BE 21	B38
7	Y IN 3H	Chroma Proc BE 21	A39
9	Y IN 4H	Chroma Proc BE 21	A40
11	Y IN 5H	Chroma Proc BE 21	B40
13	Y IN 6H	Chroma Proc BE 21	A41
15	Y IN 7H	Chroma Proc BE 21	B41
17	U/V IN 0H	Chroma Proc BE 21	A42
19	U/V IN 1H	Chroma Proc BE 21	B42
21	U/V IN 2H	Chroma Proc BE 21	A43
23	U/V IN 3H	Chroma Proc BE 21	B43
25	U/V IN 4H	Chroma Proc BE 21	A44
27	U/V IN 5H	Chroma Proc BE 21	B44
29	U/V IN 6H	Chroma Proc BE 21	A45
31	U/V IN 7H	Chroma Proc BE 21	B45
33	KEY IN 0H	Chroma Proc BE 22	A40
35	KEY IN 1H	Chroma Proc BE 22	B40
37	KEY IN 2H	Chroma Proc BE 22	A41
39	KEY IN 3H	Chroma Proc BE 22	B41
41	KEY IN 4H	Chroma Proc BE 22	A42
43	KEY IN 5H	Chroma Proc BE 22	B42
45	KEY IN 6H	Chroma Proc BE 22	A43
47	KEY IN 7H	Chroma Proc BE 22	B43
49	CLOCK IN	Chroma Proc BE 21	B46

EBU 601 INTERFACE (ECL Levels)

Pin	Function	Pin	Function
1	+ Clock	14	- Clock
2	System Ground	15	System Ground
3	+ Data 7 (MSB)	16	- Data 7 (MSB)
4	+ Data 6	17	- Data 6
5	+ Data 5	18	- Data 5
6	+ Data 4	19	- Data 4
7	+ Data 3	20	- Data 3
8	+ Data 2	21	- Data 2
9	+ Data 1	22	- Data 1
10	+ Data 0	23	- Data 0
11		24	
12		25	
13	Chassis Ground		

(3,7B)

(b) OUTPUT CHANNELS 1 - 4

The two 25-way D-Type connectors (Channel 1 and 2) provide EBU 601 standard digital video outputs. The two 50-way ribbon connectors (Channel 3 and 4) provide Quantel standard digital video outputs. These 4 outputs are routed through the I/O Expander Output card from the Coder card.

QUANTEL I/F Pin	Function	Printed Circuit Board Board	Slot	Pin
1	Y OUT 0H	Coder card	BE 25	A65
3	Y OUT 1H	Coder card	BE 25	B65
5	Y OUT 2H	Coder card	BE 25	A66
7	Y OUT 3H	Coder card	BE 25	B66
9	Y OUT 4H	Coder card	BE 25	A67
11	Y OUT 5H	Coder card	BE 25	B67
13	Y OUT 6H	Coder card	BE 25	A68
15	Y OUT 7H	Coder card	BE 25	B68
17	U/V OUT 0H	Coder card	BE 25	A70
19	U/V OUT 1H	Coder card	BE 25	B70
21	U/V OUT 2H	Coder card	BE 25	A71
23	U/V OUT 3H	Coder card	BE 25	B71
25	U/V OUT 4H	Coder card	BE 25	A72
27	U/V OUT 5H	Coder card	BE 25	B72
29	U/V OUT 6H	Coder card	BE 25	A73
31	U/V OUT 7H	Coder card	BE 25	B73
33	KEY OUT 0H	Coder card	BE 25	A61
35	KEY OUT 1H	Coder card	BE 25	B61
37	KEY OUT 2H	Coder card	BE 25	A62
39	KEY OUT 3H	Coder card	BE 25	B62
41	KEY OUT 4H	Coder card	BE 25	A63
43	KEY OUT 5H	Coder card	BE 25	B63
45	KEY OUT 6H	Coder card	BE 25	A64
47	KEY OUT 7H	Coder card	BE 25	B64
49	CLOCK OUT	O/P TIMING	BE 24	A72

EBU 601 INTERFACE (ECL Levels)

Pin	Function	Pin	Function
1	+ Clock	14	- Clock
2	System Ground	15	System Ground
3	+ Data 7 (MSB)	16	- Data 7 (MSB)
4	+ Data 6	17	- Data 6
5	+ Data 5	18	- Data 5
6	+ Data 4	19	- Data 4
7	+ Data 3	20	- Data 3
8	+ Data 2	21	- Data 2
9	+ Data 1	22	- Data 1
10	+ Data 0	23	- Data 0
11		24	
12		25	
13	Chassis Ground		

(3,7B)

(c) INPUT A

This is a 50-way ribbon connector which is used to transfer digital video from a Paintbox to the Harry system.

INPUT A Pin	Function	Printed Circuit Board Board	Slot	Pin
1	Y IN 0H	Codec card	TE 22	A11
3	Y IN 1H	Codec card	TE 22	B11
5	Y IN 2H	Codec card	TE 22	A12
7	Y IN 3H	Codec card	TE 22	B12
9	Y IN 4H	Codec card	TE 22	A13
11	Y IN 5H	Codec card	TE 22	B13
13	Y IN 6H	Codec card	TE 22	A14
15	Y IN 7H	Codec card	TE 22	B14
17	U/V IN 0H	Codec card	TE 22	A15
19	U/V IN 1H	Codec card	TE 22	B15
21	U/V IN 2H	Codec card	TE 22	A16
23	U/V IN 3H	Codec card	TE 22	B16
25	U/V IN 4H	Codec card	TE 22	A17
27	U/V IN 5H	Codec card	TE 22	B17
29	U/V IN 6H	Codec card	TE 22	A18
31	U/V IN 7H	Codec card	TE 22	B18
33	PBSTAT 3 IN	Codec card	TE 22	A35
35	PBSTAT 2 IN	Codec card	TE 22	B35
37	PBSTAT 1 IN	Codec card	TE 22	A36
39	PBSTAT 0 IN	Codec card	TE 22	B36
41	SELECT 1 OUT	Codec card	TE 22	B37
43	SELECT 0 OUT	Codec card	TE 22	A37
45	PBRFB IN	Codec card	TE 22	B20
47	PBLRST IN	Codec card	TE 22	A20
49	PBRPPCK IN	Codec card	TE 22	A19

Note: all even numbered pins on INPUT A are connected to 0 volts.

All signals are TTL levels and timed to the output side system clocks and timing signals.

(d) OUTPUT A

This is a 50-way ribbon connector which is used to transfer digital video to a Paintbox from the Harry system.

OUTPUT A Pin	Function	Printed Circuit Board Board	Slot	Pin
1	Y OUT 0H	Codec card	TE 22	A21
3	Y OUT 1H	Codec card	TE 22	B21
5	Y OUT 2H	Codec card	TE 22	A22
7	Y OUT 3H	Codec card	TE 22	B22
9	Y OUT 4H	Codec card	TE 22	A23
11	Y OUT 5H	Codec card	TE 22	B23
13	Y OUT 6H	Codec card	TE 22	A24
15	Y OUT 7H	Codec card	TE 22	B24
17	U/V OUT 0H	Codec card	TE 22	A25
19	U/V OUT 1H	Codec card	TE 22	B25
21	U/V OUT 2H	Codec card	TE 22	A26
23	U/V OUT 3H	Codec card	TE 22	B26
25	U/V OUT 4H	Codec card	TE 22	A27
27	U/V OUT 5H	Codec card	TE 22	B27
29	U/V OUT 6H	Codec card	TE 22	A28
31	U/V OUT 7H	Codec card	TE 22	B28
33		Codec card	TE 22	
35		Codec card	TE 22	
37		Codec card	TE 22	
39		Codec card	TE 22	
41		Codec card	TE 22	
43		Codec card	TE 22	
45	PBWFRST OUT	Codec card	TE 22	B30
47	PBWLRST OUT	Codec card	TE 22	A30
49	PBWPPCLK OUT	Codec card	TE 22	A29

Note: all even numbered pins on OUTPUT A are connected to 0 volts.

All signals are TTL levels and timed to the output side system clocks and timing signals.

(e) RADIAL

These are 60-way ribbon connectors which control the "Top Right", "Top Left", "Bottom Right" and "Bottom Left" Disk Drives. The Disk Controller card in each satellite section of the Harry crate provides the appropriate control for its Disk Drive:

CONNECTOR	SATELLITE	CONNECTOR
TE 08	TOP RIGHT	RADIAL TR
TE 01	TOP LEFT	RADIAL TL
BE 08	BOT RIGHT	RADIAL BR
BE 01	BOT LEFT	RADIAL BL

RADIAL BL Pins	**Function**	**Printed Circuit Board**	
		Board	**Pins**
1 & 31	TAG 1	Disk Controller	A46 & B46
2 & 32	TAG 2	Disk Controller	A45 & B45
3 & 33	TAG 3	Disk Controller	A44 & B44
4 & 34	BUS 0	Disk Controller	A43 & B43
5 & 35	BUS 1	Disk Controller	A42 & B42
6 & 36	BUS 2	Disk Controller	A41 & B41
7 & 37	BUS 3	Disk Controller	A40 & B40
8 & 38	BUS 4	Disk Controller	A38 & B38
9 & 39	BUS 5	Disk Controller	A37 & B37
10 & 40	BUS 6	Disk Controller	A36 & B36
11 & 41	BUS 7	Disk Controller	A35 & B35
12 & 42	BUS 8	Disk Controller	A34 & B34
13 & 43	BUS 9	Disk Controller	A30 & B30
14 & 44	OPEN CABLE DET	Disk Controller	A28 & B28
15 & 45	STATUS 3	Disk Controller	A27 & B27
16 & 46	STATUS 2	Disk Controller	A26 & B26
17 & 47	STATUS 1	Disk Controller	A25 & B25
18 & 48	STATUS 6	Disk Controller	A24 & B24
19 & 49	STATUS 0	Disk Controller	A23 & B23
20 & 50	STATUS 5	Disk Controller	A22 & B22
21 & 51	BUSY	Disk Controller	A21 & B21
22 & 52	UNIT SELECT TAG	Disk Controller	A20 & B20
23 & 53	UNIT SELECT 1	Disk Controller	A18 & B18
24 & 54	UNIT SELECT 2	Disk Controller	A17 & B17
25 & 55	STATUS 7	Disk Controller	A16 & B16
26 & 56	UNIT SELECT 4	Disk Controller	A15 & B15
27 & 57	TAG 5	Disk Controller	A14 & B14
28 & 58	STATUS 4	Disk Controller	A13 & B13
29	SPINDLE SEQ PICK	Disk Controller	A12
59	SPINDLE SEQ HOLD	Disk Controller	B12
30 & 60	TAG 4	Disk Controller	A11 & B11

All signals are complementary pair current drive.

(3,7B)

(f) SMD BUS

These are 60-way ribbon connectors which pass data to the "Top Right", "Top Left", "Bottom Right" and "Bottom Left" Disk Drives. The Disk Interface card in each satellite section of the Harry crate provides the appropriate parallel data for its Disk Drive:

CONNECTOR	SATELLITE	CONNECTOR
TE 09	TOP RIGHT	RADIAL TR
TE 02	TOP LEFT	RADIAL TL
BE 09	BOT RIGHT	RADIAL BR
BE 02	BOT LEFT	RADIAL BL

RADIAL BL Pins	**Function**	**Printed Circuit Board** **Board**	 **Pins**
1 & 31	ROT SYNC PULSE	Disk Interface	A46 & B46
2 & 32	UNIT SELECTED	Disk Interface	A45 & B45
3 & 33	SEEK END	Disk Interface	A44 & B44
4 & 34	INDEX	Disk Interface	A43 & B43
5 & 35	GND	Disk Interface	A42 & B42
6 & 36	SECTOR	Disk Interface	A41 & B41
7 & 37	SECTOR COMPLETE	Disk Interface	A40 & B40
8 & 38	READ DATA CHAN 0	Disk Interface	A38 & B38
9 & 39	GND	Disk Interface	A37 & B37
10 & 40	READ DATA CHAN 1	Disk Interface	A36 & B36
11 & 41	READ DATA CHAN 2	Disk Interface	A35 & B35
12 & 42	READ DATA CHAN 3	Disk Interface	A34 & B34
13 & 43	GND	Disk Interface	A30 & B30
14 & 44	READ DATA CHAN 4	Disk Interface	A28 & B28
15 & 45	READ CLK CHAN 0	Disk Interface	A27 & B27
16 & 46	READ CLK CHAN 1	Disk Interface	A26 & B26
17 & 47	GND	Disk Interface	A25 & B25
18 & 48	READ CLK CHAN 2	Disk Interface	A24 & B24
19 & 49	READ CLK CHAN 3	Disk Interface	A23 & B23
20 & 50	READ CLK CHAN 4	Disk Interface	A22 & B22
21 & 51	GND	Disk Interface	A21 & B21
22 & 52	1F WRITE CLK	Disk Interface	A20 & B20
23 & 53	WRITE DATA CHAN 0	Disk Interface	A18 & B18
24 & 54	WRITE DATA CHAN 1	Disk Interface	A17 & B17
25 & 55	GND	Disk Interface	A16 & B16
26 & 56	WRITE DATA CHAN 2	Disk Interface	A15 & B15
27 & 57	WRITE DATA CHAN 3	Disk Interface	A14 & B14
28 & 58	WRITE DATA CHAN 4	Disk Interface	A13 & B13
29 & 59	GND	Disk Interface	A12 & B12
30 & 60	WRITE CLOCK	Disk Interface	A11 & B11

All signals are complementary pair current.

(g) COMP SCSI

This is a 40-way ribbon connector which provides access to the system SCSI bus. This connector is used to connect SCSI compatible equipment (CIPHER Magnetic Tape reader) to the Harry system and for development and test purposes.

COMP SCSI Pin	Function	Printed Circuit Board Board	Slot	Pin
3	CREADL	CIO CARD	TE 27	A79
2	DATA0	CIO CARD	TE 27	A84
4	DATA1	CIO CARD	TE 27	A83
6	DATA2	CIO CARD	TE 27	A82
8	DATA3	CIO CARD	TE 27	A81
10	DATA4	CIO CARD	TE 27	A80
12	DATA5	CIO CARD	TE 27	A79
14	DATA6	CIO CARD	TE 27	A78
16	DATA7	CIO CARD	TE 27	A77
18	SPARE	CIO CARD	TE 27	A76
20	SPARE			
22	SPARE			
24	SPARE			
26	SPARE			
28	SPARE			
30	SPARE			
32	SPARE			
34	SPARE			
36	BUSY	CIO CARD	TE 27	A67
38	ACK	CIO CARD	TE 27	A66
40	RST	CIO CARD	TE 27	A65
42	MSG	CIO CARD	TE 27	A64
44	SEL	CIO CARD	TE 27	A63
46	C/D	CIO CARD	TE 27	A62
48	REQ	CIO CARD	TE 27	A61
50	I/O	CIO CARD	TE 27	A60

note: all odd numbered pins are connected to 0 volts.

SECTION 8 : INTERNAL CABLE CONNECTIONS

This section contains information relating to the Harry crate and PSU internal wiring and interconnections. This section includes the system interconnection diagrams, and the PSU circuit diagram.

3:8:1 Edge Connector Identifications

Bottom Rack Highway			Top Rack Highway		
BE01	Disk Controller	17711	TE01	Disk Controller	17711
BE02	Disk Interface	17713	TE02	Disk Interface	17713
BE03	Data Select	17730	TE03	Data Select	17730
BE04	Combiner	17732	TE04	Combiner	17732
BE05	Buffer Store 1	17715	TE05	Buffer Store 1	17715
BE06	Buffer Store 2	17715	TE06	Buffer Store 2	17715
BE07	Store Address	17716	TE07	Store Address	17716
BE08	Disk Controller	17711	TE08	Disk Controller	17711
BE09	Disk Interface	17713	TE09	Disk Interface	17713
BE10	Data Select	17730	TE10	Data Select	17730
BE11	Combiner	17732	TE11	Combiner	17732
BE12	Buffer Store 1	17715	TE12	Buffer Store 1	17715
BE13	Buffer Store 2	17715	TE13	Buffer Store 2	17715
BE14	Store Address	17716	TE14	Store Address	17716
BE15	Mux/Demux	17717	TE15	Mux/Demux	17717
BE16	Audio Proc	2003716	TE16		
BE17			TE17		
BE18			TE18	Input Switch	17718
BE19	I/P Timing	200374Y	TE19	I/O Store	17710
BE20	Chroma Filter	17673	TE20	I/O Store	17710
BE21	Chroma Proc	17654	TE21	I/O Store Control	17720
BE22	ADC	17676	TE22	Codec	2003732
BE23	RGB Input	17727	TE23	Time Code	17724
			TE24		
BE24	O/P Timing	200374Y	TE25	CPU	17601
BE25	Coder	17655	TE26	CIO	17600
BE26	RGB Output	17723	TE27	ROM/RAM	17728

Note that the 17654 card is replaced in the PAL system with 17656 and the 17673 card is replaced by 17657.

Note: E01 is the first left hand card slot in the rack.

(3,8B)

FIGURE 3.8.1 SYSTEM INTERCONNECTION DIAGRAM

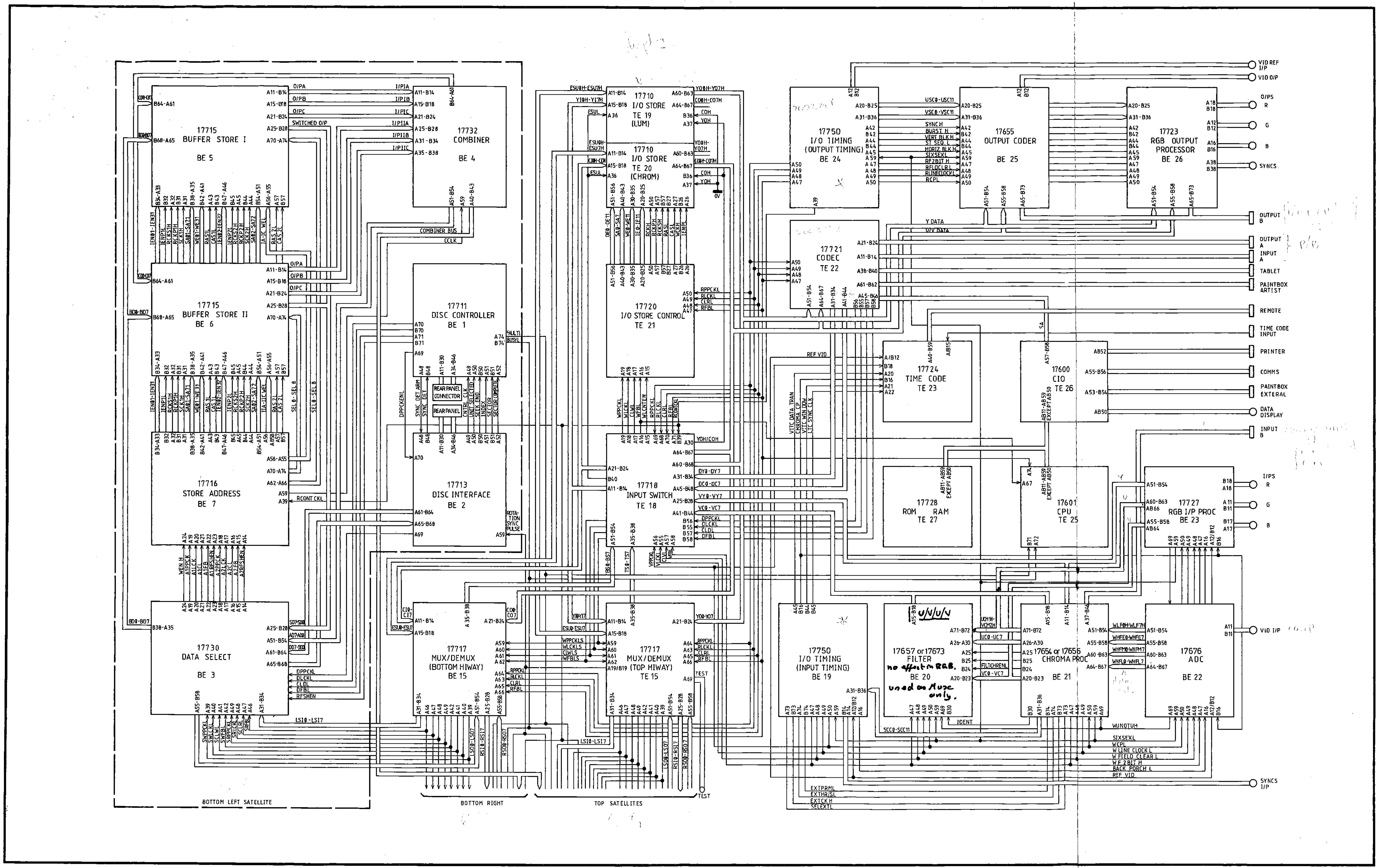
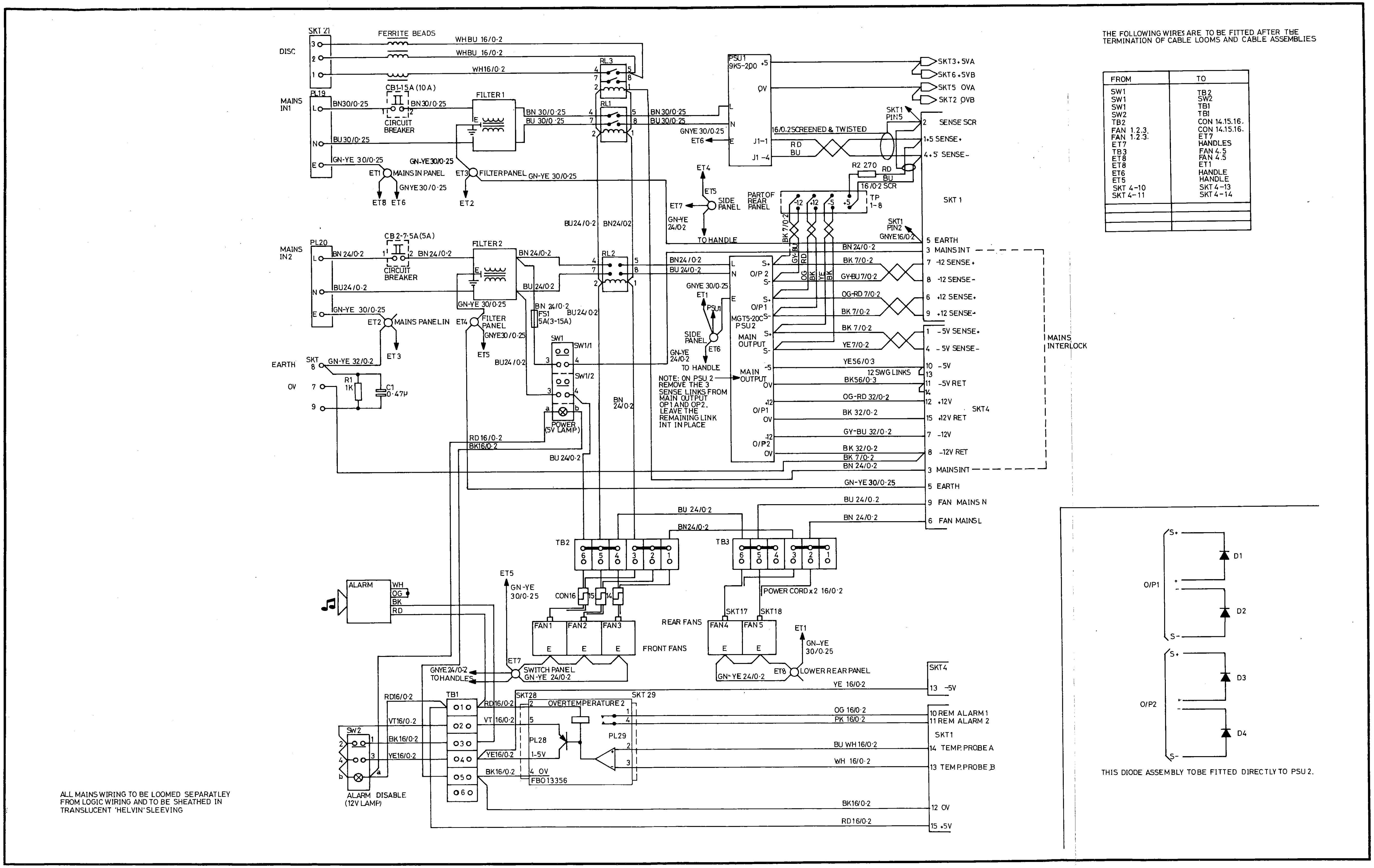


FIGURE 3.8.2 POWER SUPPLY CIRCUIT DIAGRAM 1



THE FOLLOWING WIRES ARE TO BE FITTED AFTER THE TERMINATION OF CABLE LOOMS AND CABLE ASSEMBLIES

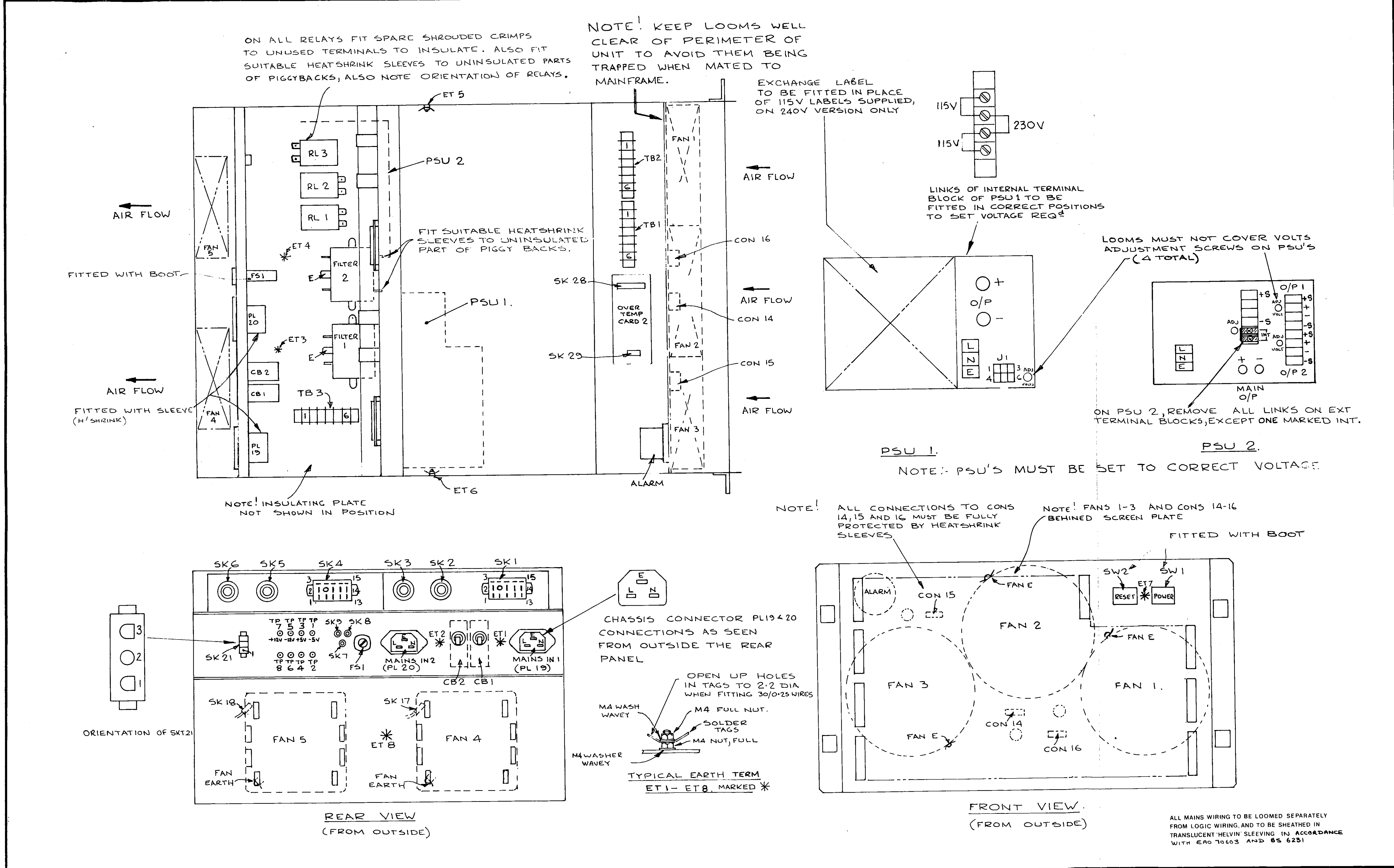
FROM	TO
SW1	TB2
SW1	SW2
SW1	TB1
SW2	TB1
TB2	CON 14.15.16.
FAN 1.2.3.	CON 14.15.16.
FAN 1.2.3.	ET7
ET7	HANDLES
TB3	FAN 4.5
ET8	FAN 4.5
ET8	ET1
ET6	HANDLE
ET5	HANDLE
SKT 4-10	SKT 4-13
SKT 4-11	SKT 4-14

NOTE: ON PSU 2 REMOVE THE 3 SENSE LINKS FROM MAIN OUTPUT OP1 AND OP2. LEAVE THE REMAINING LINK INT IN PLACE

THIS DIODE ASSEMBLY TOBE FITTED DIRECTLY TO PSU 2.

ALL MAINS WIRING TO BE LOOMED SEPARATLEY FROM LOGIC WIRING AND TO BE SHEATHED IN TRANSLUCENT 'HELVIN' SLEEVING

FIGURE 3.8.3 POWER SUPPLY CIRCUIT DIAGRAM 2



ON ALL RELAYS FIT SPARE SHROUDED CRIMPS TO UNUSED TERMINALS TO INSULATE. ALSO FIT SUITABLE HEATSHRINK SLEEVES TO UNINSULATED PARTS OF PIGGYBACKS, ALSO NOTE ORIENTATION OF RELAYS.

NOTE! KEEP LOOMS WELL CLEAR OF PERIMETER OF UNIT TO AVOID THEM BEING TRAPPED WHEN MATED TO MAINFRAME.

EXCHANGE LABEL TO BE FITTED IN PLACE OF 115V LABELS SUPPLIED, ON 240V VERSION ONLY

LINKS OF INTERNAL TERMINAL BLOCK OF PSU 1 TO BE FITTED IN CORRECT POSITIONS TO SET VOLTAGE REQ^d

LOOMS MUST NOT COVER VOLTS ADJUSTMENT SCREWS ON PSU'S (4 TOTAL)

FIT SUITABLE HEATSHRINK SLEEVES TO UNINSULATED PART OF PIGGY BACKS.

ON PSU 2, REMOVE ALL LINKS ON EXT TERMINAL BLOCKS, EXCEPT ONE MARKED INT.

NOTE! INSULATING PLATE NOT SHOWN IN POSITION

NOTE:- PSU'S MUST BE SET TO CORRECT VOLTAGE

NOTE! ALL CONNECTIONS TO CONS 14, 15 AND 16 MUST BE FULLY PROTECTED BY HEATSHRINK SLEEVES

NOTE! FANS 1-3 AND CONS 14-16 BEHIND SCREEN PLATE

CHASSIS CONNECTOR PL19 & 20 CONNECTIONS AS SEEN FROM OUTSIDE THE REAR PANEL

OPEN UP HOLES IN TAGS TO 2·2 DIA WHEN FITTING 30/0·25 WIRES

ALL MAINS WIRING TO BE LOOMED SEPARATELY FROM LOGIC WIRING, AND TO BE SHEATHED IN TRANSLUCENT 'HELVIN' SLEEVING IN ACCORDANCE WITH EAO 70603 AND BS 6231

DCR 7700/1 HARRY
INSTALLATION AND SERVICE MANUAL
CHAPTER 4 : CIRCUIT DESCRIPTIONS

This chapter contains the circuit description, the component layout, the block diagram and the circuit diagrams for the following crate mounted Printed circuits:

4:1:1 17600 CIO card 137
4:2:1 17601 CPU card 145
4:3:1 17654 Chroma Processor card (NTSC) 153
4:4:1 17655 Coder card 159
4:5:1 17656 Chroma Processor card (PAL) 171
4:6:1 17657 Chroma Filter card (PAL) 181
4:7:1 17673 Chroma Filter card (NTSC) 189
4:8:1 17676 ADC card 195
4:9:1 17710 I/O Store card 203
4:10:1 17711 Disk Controller card 209
4:11:1 17713 Disk Interface card 217
4:12:1 17715 Buffer Store card 223
4:13:1 17716 Store Address card 231
4:14:1 17717 Mux/Demux card 239
4:15:1 17718 Input Switch card 245
4:16:1 17720 I/O Store Control card 253
4:17:1 2003732 Codec card 261
4:18:1 17723 RGB Output card 267
4:19:1 17724 Time Code card 277
4:20:1 17727 RGB Input card 287
4:21:1 17728 ROM/RAM card 299
4:22:1 17730 Data Select card 305
4:23:1 17732 Combiner card 311
4:24:1 200374Y I/O Timing card 319
4:25:1 2003716 Audio Processor card 329

COMPUTER INPUT OUTPUT CARD 17600B

4:1:1 Function

The CIO card performs four major functions within the system computer, in conjunction with the CPU card:

Serial Interfacing to external peripherals.

DMA control of data transfer between the system computer and peripherals.

SCSI Disc interface.

VDU Graphics display providing the Data Display for the system.

4:1:2 Circuit Description

(a) SDLC INTERFACE

The control station SDLC protocol is executed by the CPU system software and the serial interface devices KE and ME (Z8030). These serial interfaces connect the control stations to the CPU. KE and ME are address mapped, and are accessed when the PAL DH decodes the relevant addresses.

SE, RH, RG and the PAL PG synchronize data transfer to and from the CPU, and produce the relevant timing signals for KE and ME. Data is transferred via the bi-directional buffers GH and OG under the control of PAL PG.

(b) SCSI INTERFACE

The SCSI interface controller EB (NCR5385) controls the interface between the CPU and Winchester Disc drive. The PAL DF controls the interfacing between the CPU and EB, and the direction of data through the buffers CG and GG. When the Winchester Disc is accessed, address and data are enabled onto the system computer bus by AA and CA.

(c) DMA CONTROLLERS

The DMA controllers IG and MG provide eight channels of DMA control, which are allocated to the following peripherals:

Controller MG

0	SCSI controller
1	Control Box transmit
2	Control Box receive
3	External (not used)

Controller IG

0	SDLC loop transmit
1	Auxiliary serial transmit
2	Auxiliary serial receive
3	SDLC loop receive

The DMA controllers are linked to the CPU data bus via the Bi-directional buffers DG and FG. The registers EG and FH hold the addresses generated by the DMA controllers, when a DMA is progress. These registers are controlled by the DMA controllers, which also determine the direction of the DTACK signals, and the CPU card data buffers.

(d) VDU GRAPHICS DISPLAY (Not Used at Present)

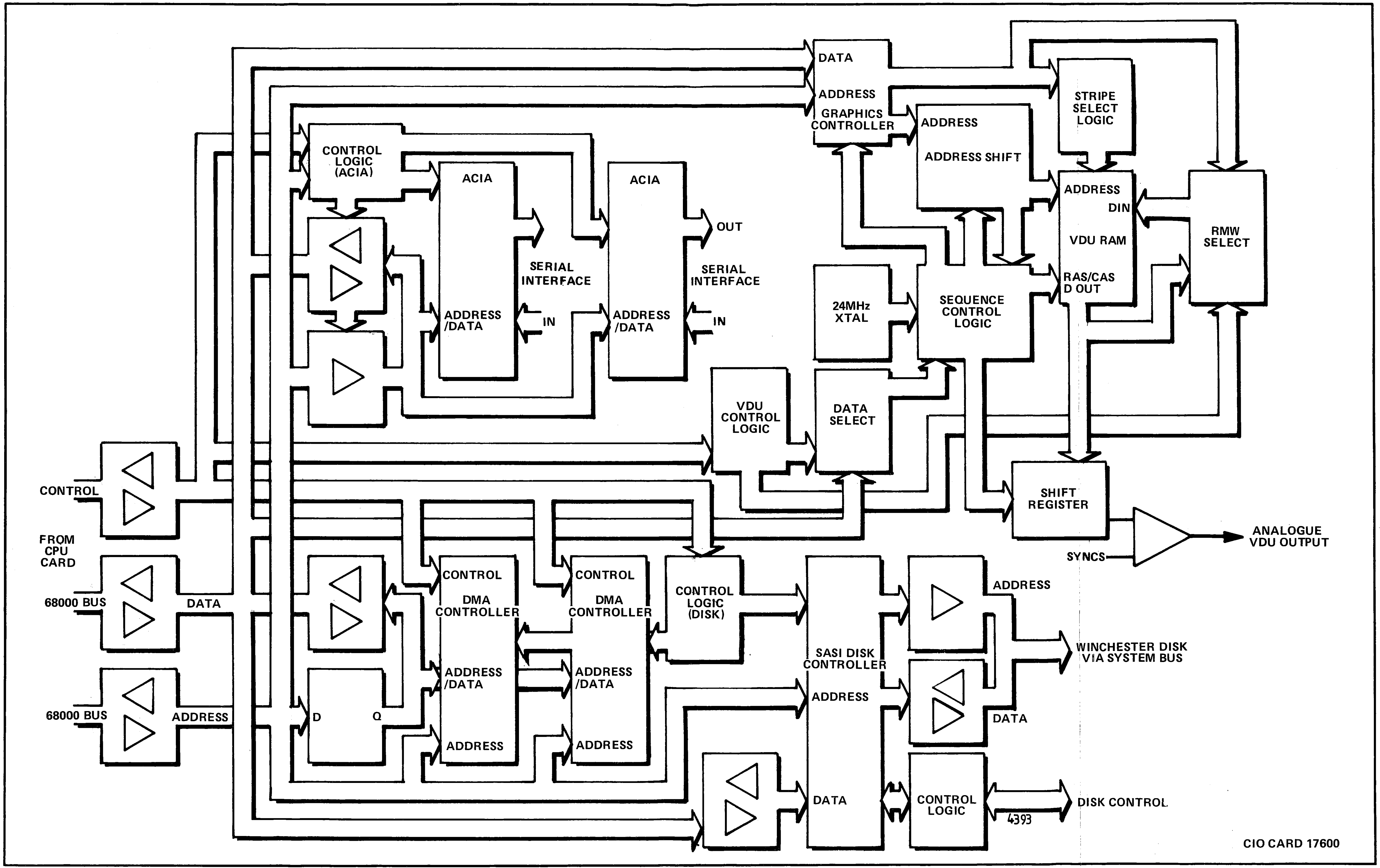
The VDU display produces a video output which is constructed from two Pages of 512 pixels by 512 lines. Both pages are used; one written while the other is displayed. The VDU is based around the VDU controller IE (EF9367).

The 24 MHz clocks from the crystal oscillator GC are divided down by the counter FE, whose output is decoded by the PAL FB to provide the timing signals for the VDU circuit.

The selector IB multiplexes the most significant addresses to control which page of the VDU is written and which page is displayed. The selector circuit FF and GF shifts the addresses depending on whether the Read or Write processes are taking place. The shifted addresses are buffered by DA into the address input of the RAMs.

The RAMs are controlled by OB and SB, which determine which are to be Written into from the selector RE. Data is Read from all 16 RAMs and loaded into the shift registers HB and PB, then shifted out at video rate to produce the VDU display data. This data is inverted by DF and passed to the amplifier circuit TR1, TR2 and associated components, where video sync pulses are added.

(4,1B)
FIGURE 4.1.1 17600B CIO BLOCK DIAGRAM



(4,1B)

FIGURE 4.1.2 17600B CIO LAYOUT

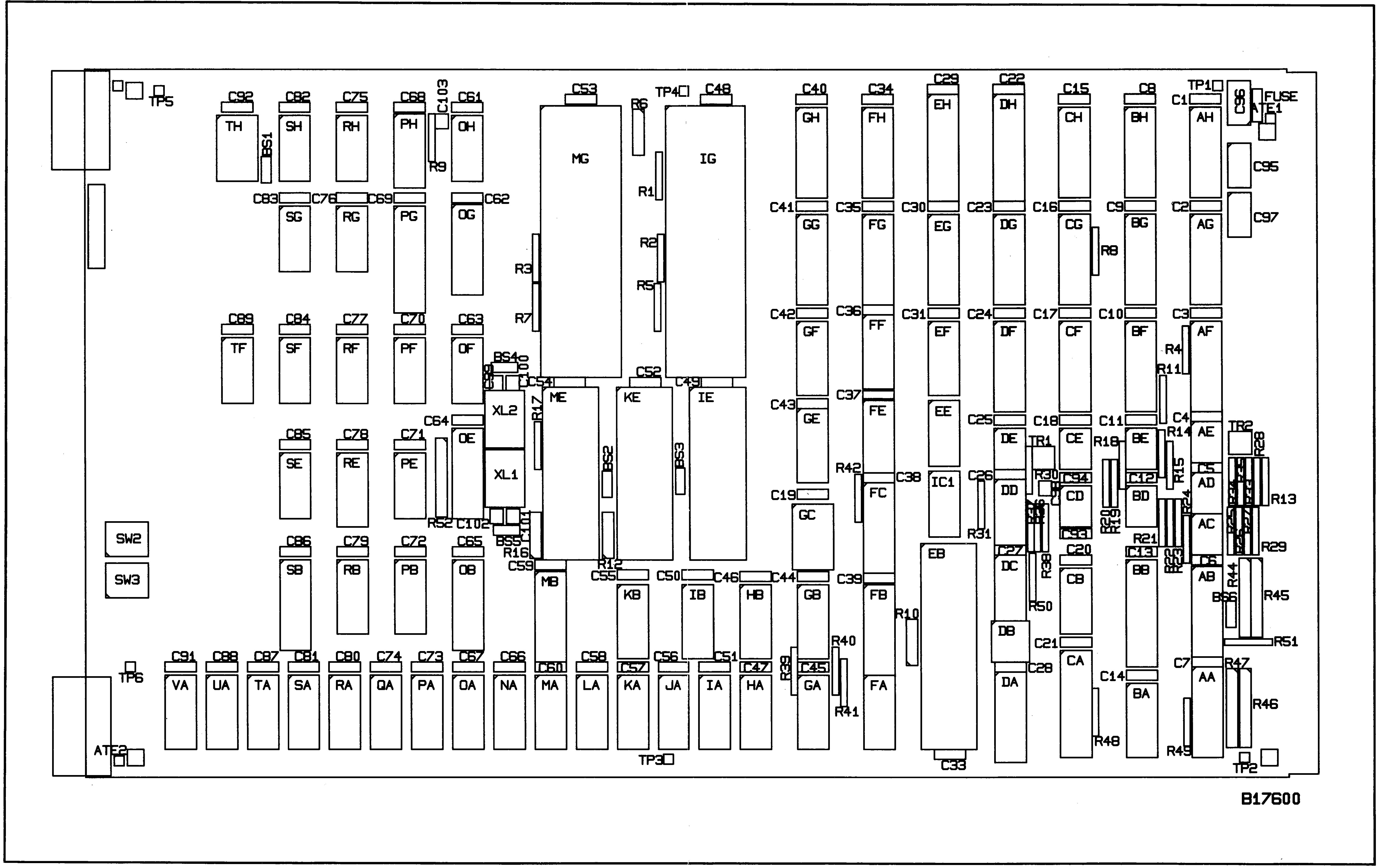
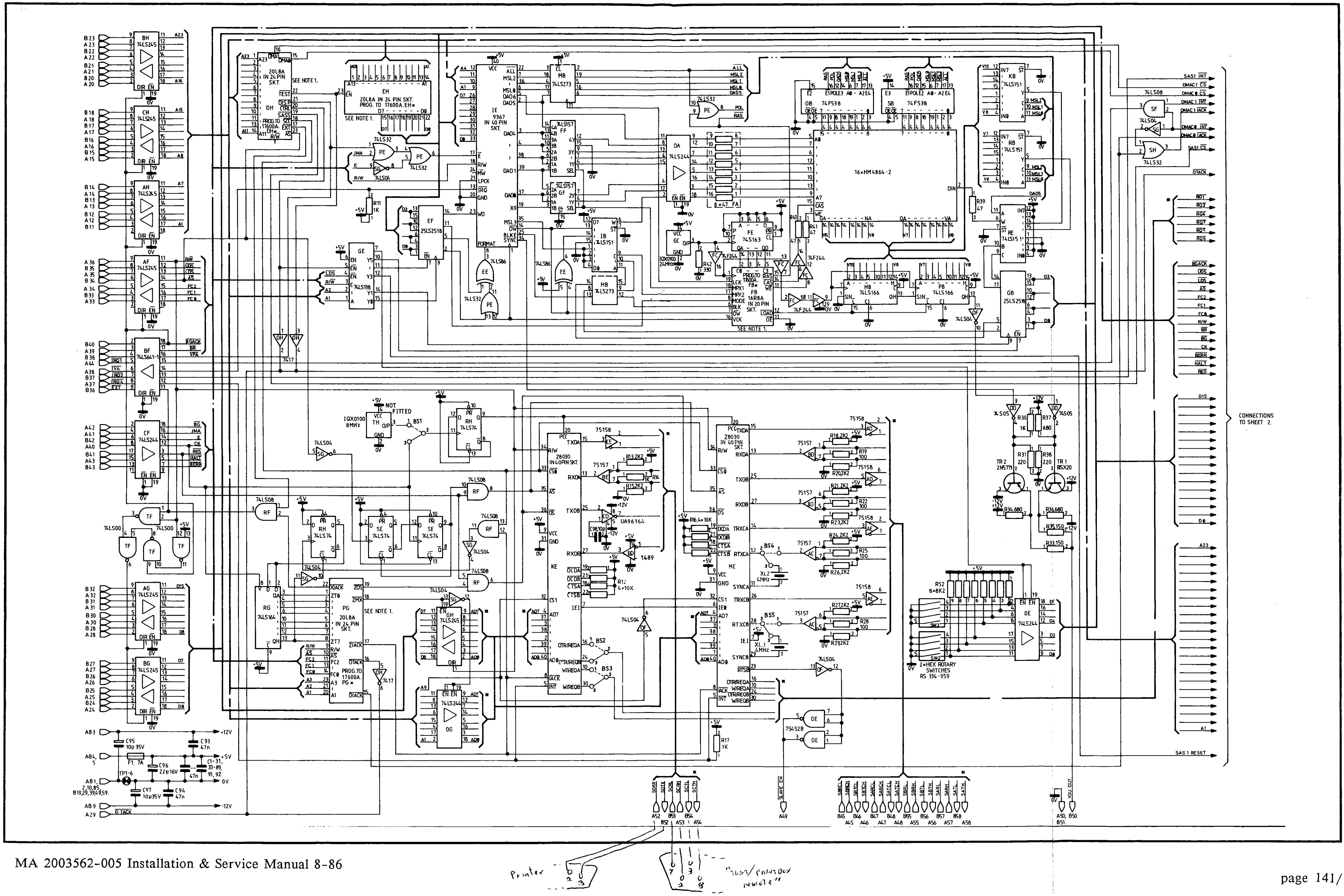
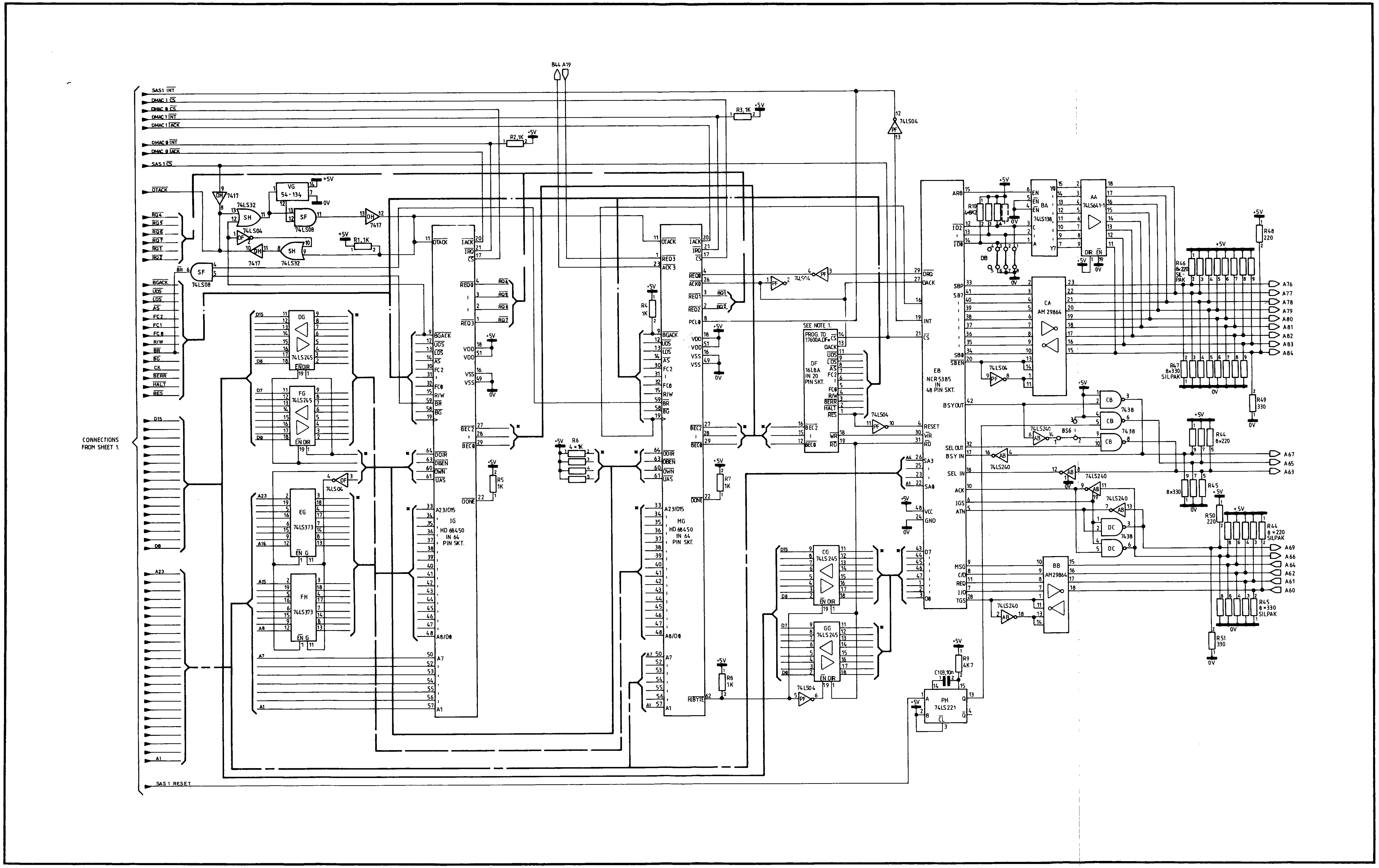


FIGURE 4.1.3 17600B CIO CIRCUIT 1



(4,1B)
FIGURE 4.1.4 17600B CIO CIRCUIT 2



CPU CARD 17601C

4:2:1 Function

The CPU card, the CIO card and the RAM/ROM card form the Harry system computer. The CPU card is a 68010 based Micro Processor computer with a Floating Point processor. The card also carries various interfacing circuitry and the Micro Processor's memory. The system operating software is held in the RAM/ROM card and is loaded into the CPU Ram on power up or system Reset.

4:2:2 Circuit Description

(a) POWER UP RESET

On power up or CPU reset, PA generates a reset pulse which is sent to the CD (68010). This causes CD to enter its startup mode and then start executing instructions.

The first 4 memory locations reside in the Monitor EPROMs EE and FE, whose addresses are overlaid onto the RAM address map. On reset the EPROMs are Read to provide startup and initializing values for the micro processor.

On power up the monitor program runs a series of "self tests" on the CPU card, and when finished produces an output on the HEX displays.

(b) TIMING CIRCUITRY

The 16 MHz oscillator XL1 provides the computer master clocks, which are passed to OC, which produces an 8 MHz clock for the CPU card.

DTACK is a signal received by the 68010 which determines whether the device addressed has completed it's data transfer. The PAL CC generates DTACK timing signals for devices which do not generate DTACK ie. EPROM, Static RAM, the system bus, and the Floating Point Processor. These signals are produced by gating Address strobes from DD together with the relevant Address decodes.

UDS and LDS are data strobes, which remain low during data transfer to or from the 68010. The counter MD monitors the duration of the transfer, and should it exceed 2048 clock cycles, sends a low to pin 22 of CD.

(c) INTERRUPT CIRCUITRY

The PAL CC acts as a priority encoder, which generates an interrupt code determined by the priority level of interrupts received. When the 68010 receives an interrupt it responds by setting the function code to "7" and reflects the interrupt level on the addresses A1 to A3.

The highest priority interrupt is generated by the black push button on the CPU card. The next highest interrupt is generated by the "Power Fail" circuit TR2, TR3, D1 and GF. The following is a summary of the sources and the interrupt level:

level	Source	Board	Comments
7	Black button	CPU	diagnostics
6	Power Fail	CPU	
5	WB 6522	CPU	Field interrupts
4	Serial Ports	CIO	
3	CA 68901	CPU	Console port
2	SCSI interface	CIO	Disc interface
1	DMA controllers	CIO	

(d) SERIAL I/O

Serial I/O is provided by the multi-function device CA (68901). This provides a serial interface to the computer via the 10-way connector mounted on the front of the board. This serial interface has Auto baud rate selection which is achieved by using the "Break" and "Space" keys on the VDU/Terminal connected. This serial interface is normally only used for Test and Servicing purposes.

(e) DISPLAYS & SWITCHES

The VIA WB interfaces the switches and displays on the board to the 68010. The HEX displays are used to display the status of the computer whilst the system is under "self test". The top Hex switch, mounted on the front of the CPU, is used to select the software file which is to be automatically loaded from the Winchester Disc on power up or Reset. See Software Maintenance for details of switch settings.

(f) STATIC RAM

EF and FF provide 16K of non-volatile memory, which is supplied with a backup power source. This is provided by BAT1. This battery source is used when the power fail circuit TR1, TR5, D5 and GF detects a voltage drop.

(g) REAL TIME CLOCK

FA (MC146818) provides a real time clock for the CPU. This is also powered by the battery backup. The clock device FA uses a multiplexed address/data bus which is interfaced to the 68010 using a 6800 style bus access. The buffer EB enables the address bus onto the address/data lines of FA, and JD produces the address strobe. EB is subsequently disabled and the data from EA is enabled onto the address/data lines of FA.

(h) DYNAMIC RAM

The PAL FD decodes the address bus and produces a Row address for the 4 rows of Dynamic RAMs. When an access request is sent a low from FD appears on KC 2. If the RAM controller is not busy, KC 3 will be low and KC 1 will produce a positive edge. This clocks PC to produce a low state to start an access cycle. The negative edge from PC is propagated down the delay line RC, which produces the various RAS and CAS signals for the RAMs. A delay tap is fed back to PC to set pin 6 high; defining the delay line pulse width. ID determines which row is to be addressed by sending the RAS signal only to the required row.

The RAMs are refreshed by the CAS signals from the Refresh logic OB, PC, MC and KC. These refresh CAS signals are combined in PB with the address CAS signals,and passed to the RAMs. Refresh requests are produced by OC and occur every 16 micro seconds.

RD and TD buffer and enable the output from the RAMs onto the data bus.

(i) FLOATING POINT PROCESSOR

TB (NS16081) is used for floating point calculations, which are carried out at two address locations. These addresses are decoded by GE, which provides the appropriate enables and read/write signals for TB. The delay line YA and the associated circuitry produces a suitable data strobe for the floating point processor. The writing to and reading from the floating point processor is controlled by the circuit consisting of GE, FC, GC, HC and TA.

(j) SYSTEM BUS INTERFACE

The system bus is a parallel interface which is used to transfer data to and from the printed circuit boards within the system. The system bus consists of the following signals:

i. AD0 to AD15 pins A75 to B83

This is the multiplexed Address/data bus which is tracked to all cards along the highway.

ii. STROBEL pin B84

This is a negative going pulse used to strobe the address/data to and from the address/data bus and the cards.

iii. ADDRL pin A84

When low this indicates an address on the Address/data bus.

iv. READL pin A79

When low this indicates reading from Address/data bus. When the Address/data bus is not in use AD0 to AD15 are tri-stated into high impedance operation.

The PAL FD decodes the CPU address bus and determines when the system bus is accessed. The address to be sent is clocked into the registers BA and BB, and enabled onto the system bus. The delay line IC and associated circuitry produces the appropriate strobes and enables for the system bus.

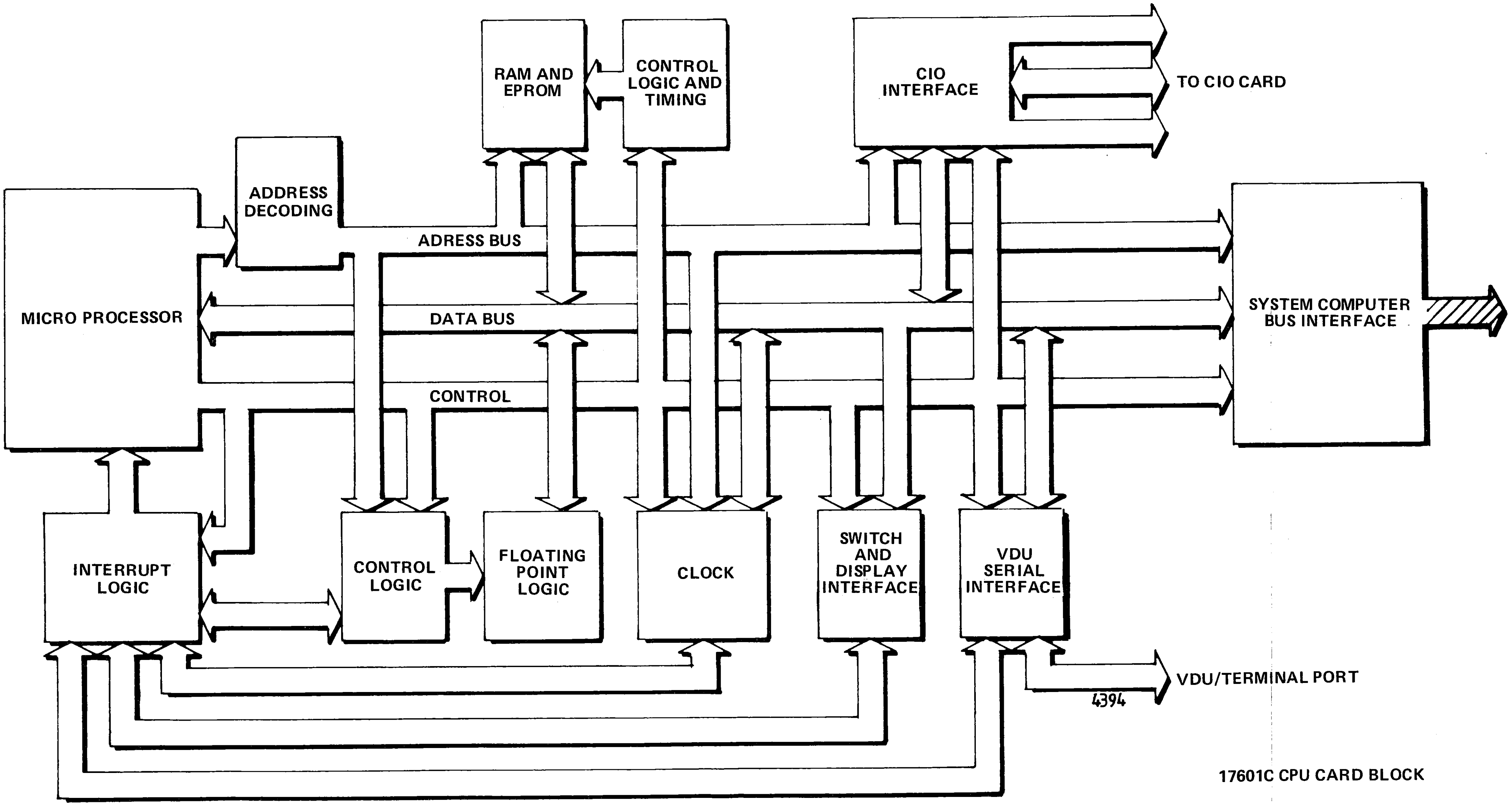
Data to be sent to the system bus is clocked into AA and AB, and then tri-stated onto the system bus, controlled by GC, HB and IC. When data is read from the system bus it is buffered by AA and AB onto the CPU data bus.

(k) EXTERNAL INTERFACE

The 68010 address, data and control lines are buffered by AC, AD, AE, AF and BF and passed to the CIO card. These lines are also buffered by BC, BD and BE, and passed to the Computer Interface card, mounted in the rear of the crate, which provides the System Bus connection.

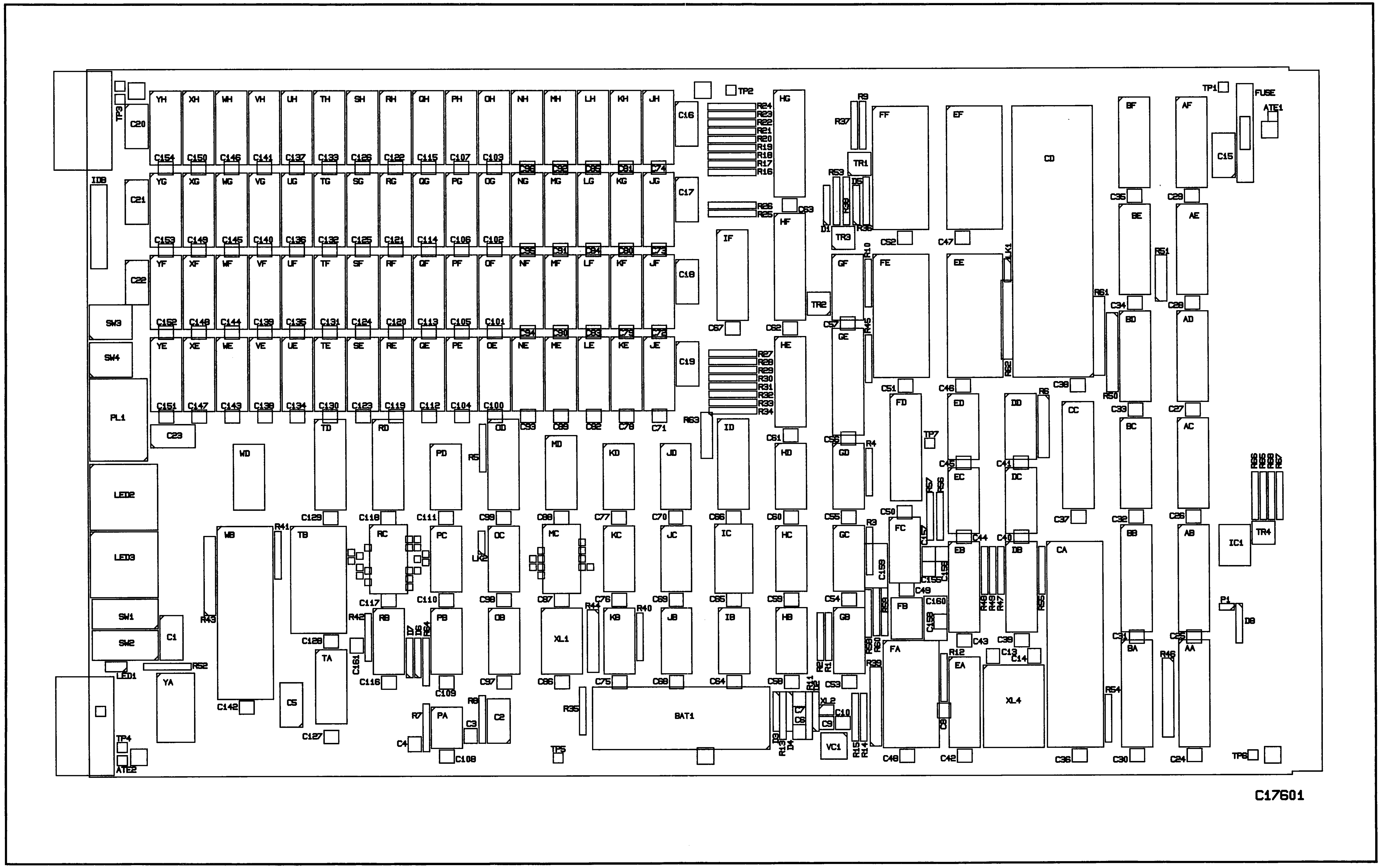
(4,2C)

FIGURE 4.2.1 17601C CPU BLOCK DIAGRAM



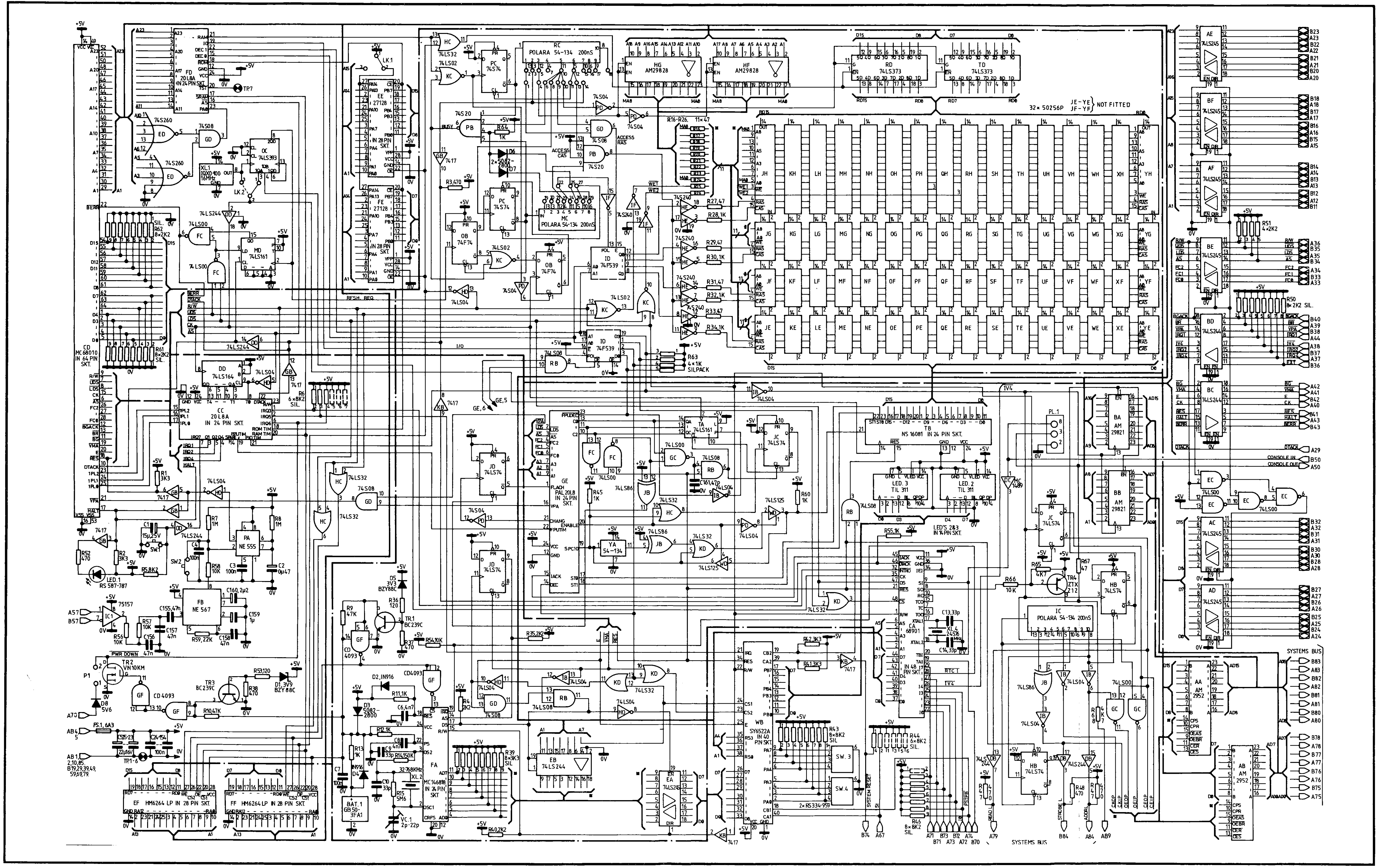
17601C CPU CARD BLOCK

(4,2C)
FIGURE 4.2.2 17601C CPU LAYOUT



(4,2C)

FIGURE 4.2.3 17601C CPU CIRCUIT



NTSC CHROMA PROCESSOR CARD 17654C

4:3:1 Function

This card in-conjunction with the ADC card forms the "Adaptive Comb Filter" and decoder of the system. This provides wide-band combed Luminance, and demodulated "U" and "V" components.

The Chroma Proc card accepts Middle-LF Luminance (1H delayed), and Early, Middle and Late-HF Luminance + Chrominance. The Input Timing card provides data used to produce digital U and V subcarriers; used to demodulate the Combed Chrominance data.

The Chroma Proc card uses the following methods to produce correctly Combed Chrominance and Luminance data:

Combed Chrominance:

Middle (HF+CHR)-[Early (HF+CHR) + Late (HF+CHR)]

HF Luminance:

(Combed CHR)-Middle (HF+CHR)

Combed Luminance:

Middle (LF Luminance)+(HF Luminance)

"Comb Fail":

Late (HF+CHR)-Early (HF+CHR)

When "Comb Fail" occurs the Chrominance output of the "Comb", becomes the Middle (HF+CHR) data, and the Combed Luminance Output becomes the Middle (LF Luminance).

4:3:2 Circuit Description

(a) COMBED CHROMINANCE PATH

Early and Late HF+CHR data is added by BB and AB, then clocked through the registers DD and EB, and through the inverting register ED, into the adder circuit FD and GC.

Middle HF+CHR data is buffered by BC, and clocked through the registers CC and EC into the adder circuit FD and GC, to produce Combed Chrominance. This Chrominance is then clocked through the pipe line registers ID, GD and GF into the multipliers IF and HF.

(b) HF LUMINANCE PATH

Chrominance data from the adder circuit FD and GC is passed to the adder HC and JD, where Middle HF+CHR, inverted by FC, is added to produce HF Luminance. This HF Luminance data is clocked through the register IC into the scaling proms JC and KC. The scaled output of these proms is clocked through the registers LC and EB into the adder LD, HC and ND.

(c) COMBED LUMINANCE PATH

Combed HF Luminance data from LC and EB, and Middle LF Luminance from HA (buffered by AD) is added in the adder circuit LD, NC and ND, to produce wide-band Luminance. This Luminance is range limited by the selectors PD and PC, and then clocked through the pipe line registers PA, NA and AF, to be passed to the Input Switch card.

(d) COMB FAIL CIRCUIT

Early HF+CHR data, inverted by CB, and Late HF+CHR, are added by DB and DC, then clocked through the registers HB and EB into the "Thresh Hold" prom IB. This prom provides a flag which is stretched by JB and KB to produce a disable signal, which turns off ID and enables HD. HD then outputs Middle HF+CHR data through the Chrominance path, and with the output of JC and KC at zero, Middle LF Luminance is produced at the output of the adder circuit LD, NC and ND.

(e) CHROMINANCE DEMODULATOR CIRCUIT

Combed Chrominance data from GF is passed to the multipliers IF and HF, where it is demodulated by the U and V subcarriers; generated by the proms NF, LF and KF (for U), and PF, QF and JF (for V). These proms are supplied with a rotational picture point count provided by the Input Timing card; clocked through the registers AE and BE.

The U and V base-band signals produced by the multipliers IF and HF, are buffered by EE and FF (for U), and EF and FF (for V), and then passed to the Chroma Filter card.

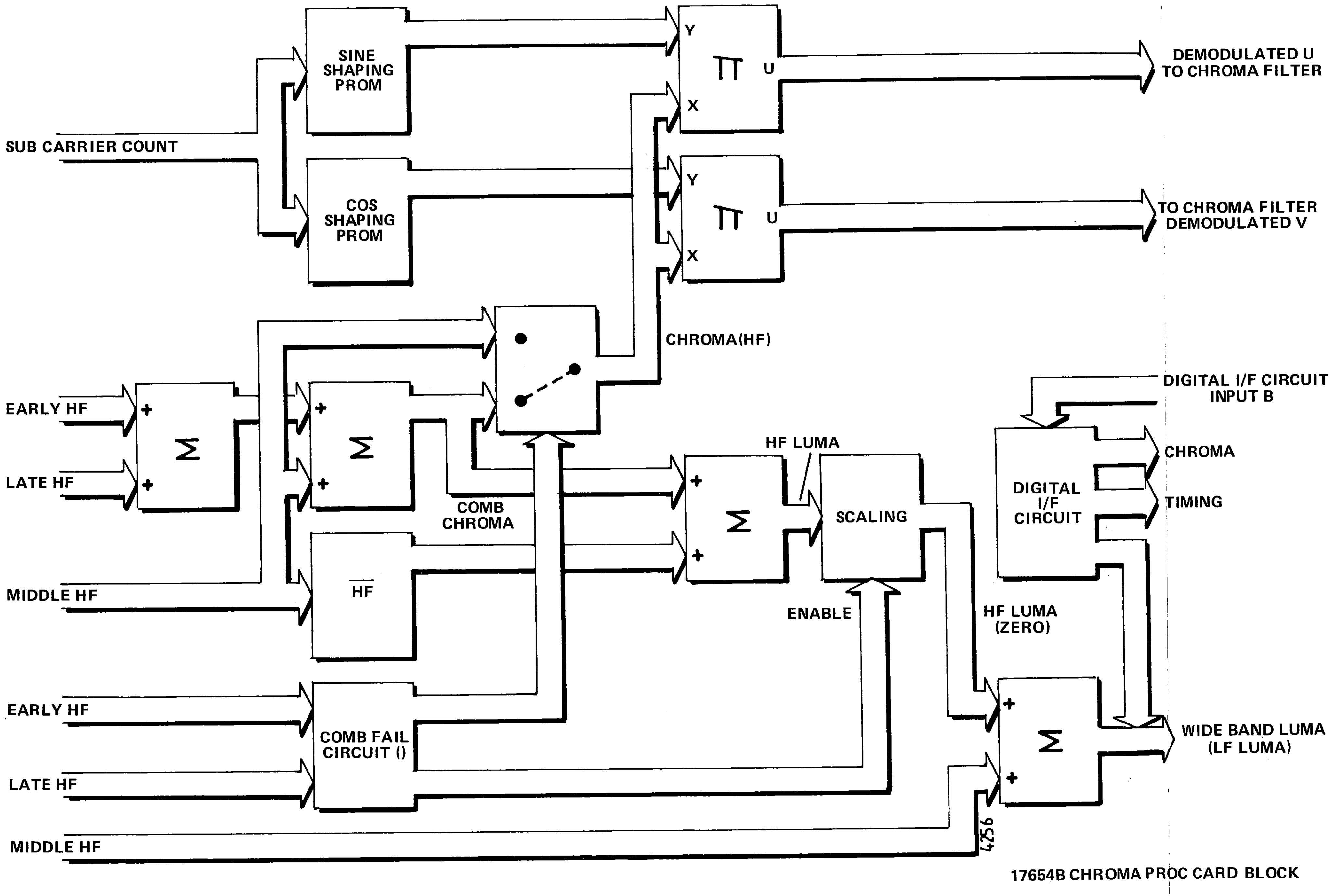
(f) DIGITAL INTERFACE CIRCUIT

Luminance and U/V data from the "INPUT B" connector (on the back panel), are buffered by CD and CE, then clocked through the registers FB and DE, and FA and CF. These output when enabled by the computer bus decode circuit, and the PAL LB subsequently decodes the data sync-words from the Luminance data. This provides the appropriate timing signals required by the Input Timing card when Digital input video is selected.

(g) COMPUTER BUS DECODE CIRCUIT

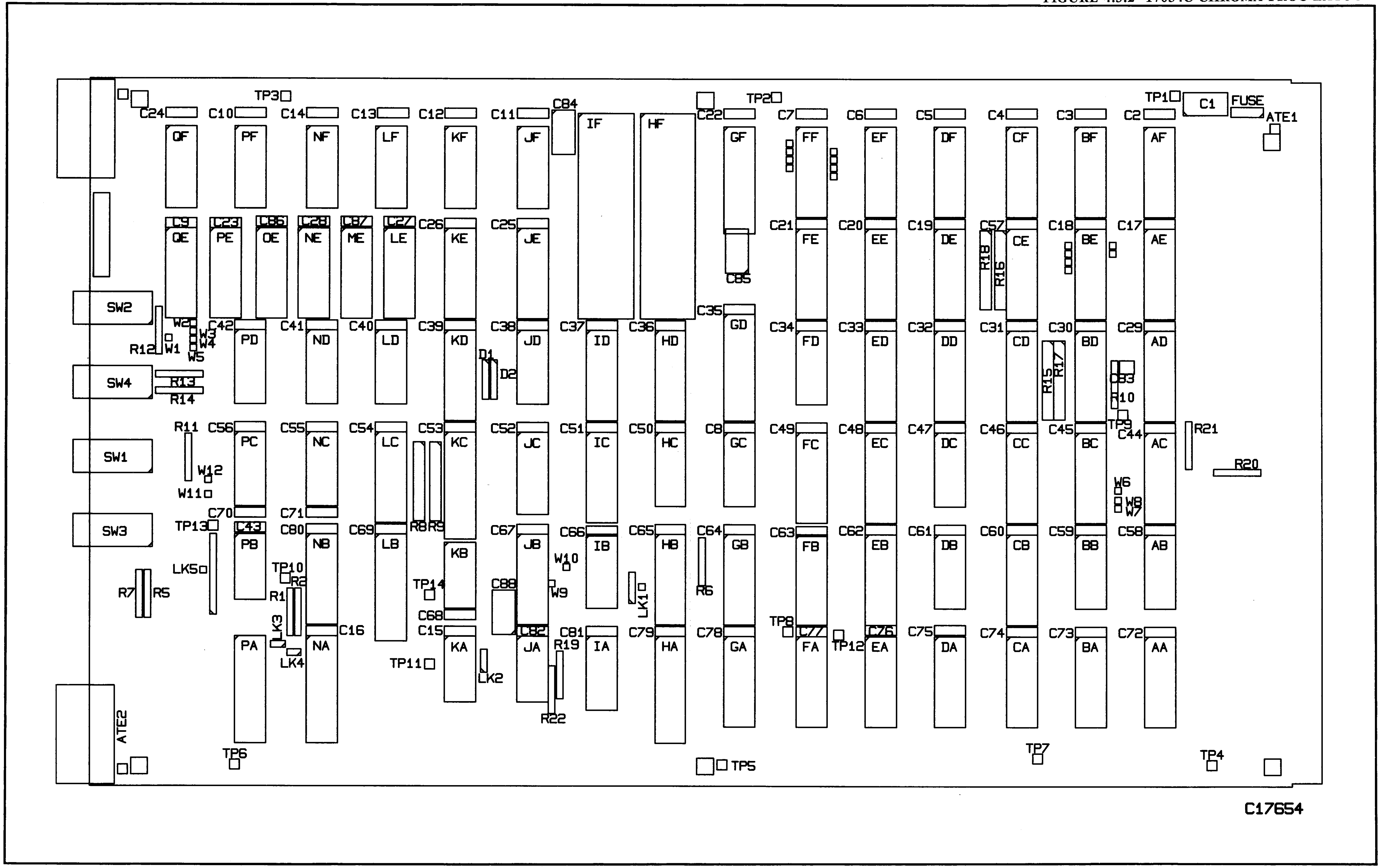
The system computer bus is buffered by BA and AA, then passed to the bus decoder-PALs CA and GB, which provide the necessary enables for the computer controlled circuitry on this card.

(4,3C)
FIGURE 4.3.1 17654C CHROMA PROC BLOCK DIAGRAM



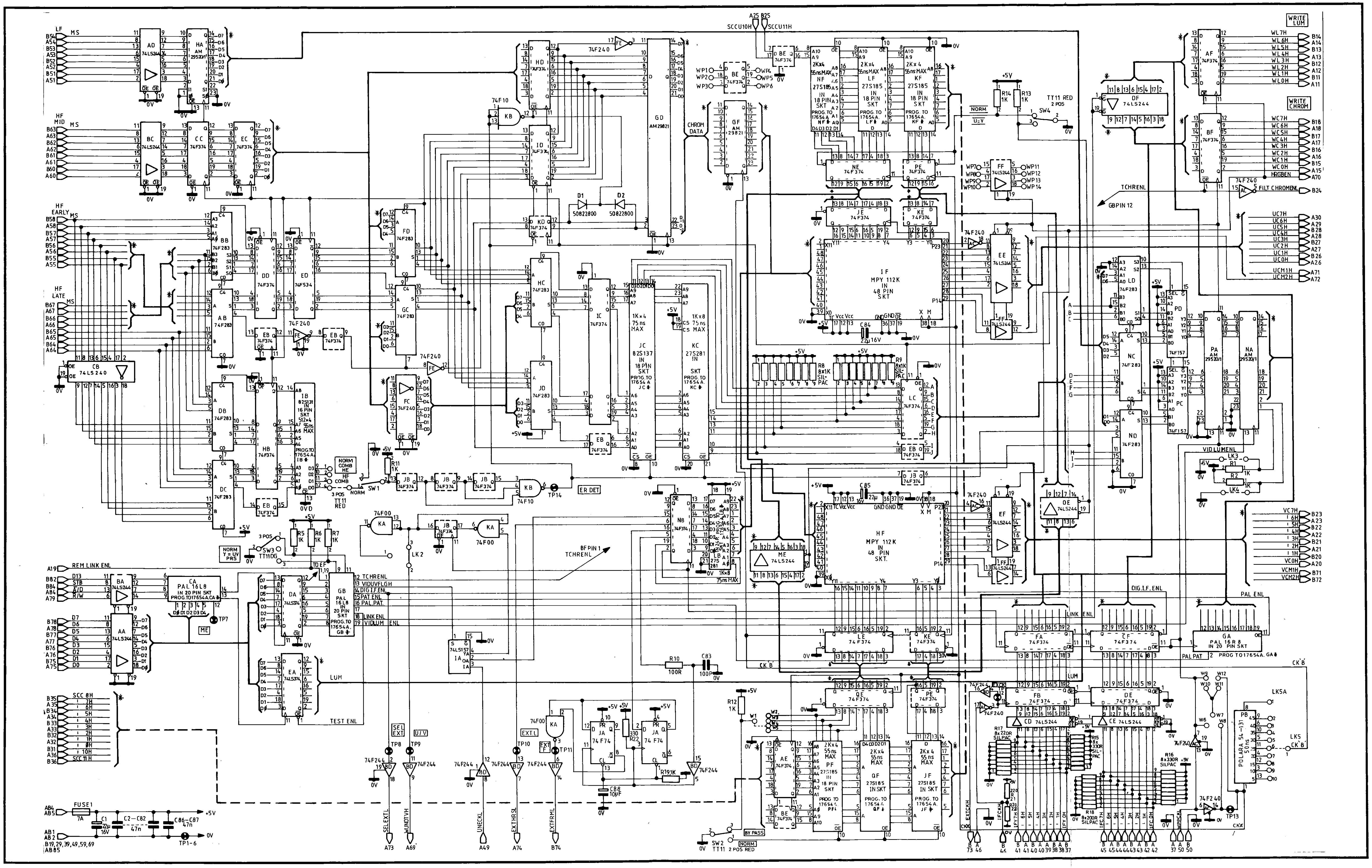
17654B CHROMA PROC CARD BLOCK

FIGURE 4.3.2 17654C CHROMA PROC LAYOUT



(4,3C)

FIGURE 4.3.3 17654C CHROMA PROC CIRCUIT



CODER CARD 17655C

4:4:1 Function

The main function of this card is to take the Luminance and U/V data from the output from the Output Store, and to digitally Encode them to produce the analogue Coded video output.

The U/V data is de-multiplexed and digitally blanked before having burst added. The "U" and "V" are then modulated with digital subcarriers from the Output Timing card.

The Luminance data is digitally blanked and has sync pulses added prior to conversion back to analogue. The analogue Luminance and the analogue Chrominance signals are then summed to produce the composite Coded Output signal.

4:4:2 Circuit Description

(a) LUMINANCE DATA PATH

Luminance data from the I/O Store is buffered by AC, and clocked through the register IB into the $\sin^2$ blanking proms KC and JC. These proms produce a $\sin^2$ blanking edge to the Luminance data, when the positive and negative edges of the R BLANK signal occur on A43. The counter ME counts up and down through the 8 states in all the $\sin^2$ blanking proms, which changes the amplitude of the data passing through them.

The output of the $\sin^2$ proms KC and JC, and the output from the sync prom LC are tri-stated onto the common Luminance and sync path; controlled by the R VIDEO/BLANK signal on A41. The prom LC produces a shaped sync pulse edge, when a negative or positive edge occurs on the R SYNC signal on A42. The counter LA counts up and down through the 8 states in the prom LC, which produces the appropriate values for the sync edge.

The R BLANK/VIDEO signal appropriately delayed becomes the MSB of the Luminance data passed to the DAC PB. This makes the top 255 levels of the data the luminance, and the bottom 255 levels the sync.

The Luminance/sync data is delayed through the pipe line registers NC, PA and LE (LSB), to match the Chrominance path delay. The delayed Luminance/sync data is then converted to analogue by the DAC PB before the Luminance and Chrominance signals are added.

(4,4C)

(b) CHROMINANCE DATA PATH

Multiplexed U and V data from the I/O Store is buffered by AB, and passed to the de-multiplexer and interpolator circuit. U and V data from AB is clocked through the registers DA and EA (which provides delayed U and V data), into the adder circuit EB and HA. This adder produces alternate samples of interpolated U and V. The interpolated data is passed to the data selector circuits IC and JA (for U data), and IE and KA (for V data), where selection between normal and interpolated data is made.

The continuous U and V data produced, is passed to the $\sin^2$ blanking proms ID and HD (for U), and GC and HC (for V), which produces a $\sin^2$ blanking edge to the data, when a positive or negative edge occurs on the R BLANK signal.

The outputs from the $\sin^2$ blanking proms, and the outputs from the burst shape proms CD (for U) and DD (for V) are tri-stated onto the U and V data paths; controlled by the R VIDEO/BLANK signal.

The proms CD and DD produce U and V shaped burst data when positive and negative edges occur on the R BURST H signal on B42. The counter KD counts up and down through the 8 states in the burst shape proms, to produce the correct burst shape and rise times.

(c) U MODULATOR

The output from the U blanking proms ID and HD is clocked through the registers GD and GF into the multiplier FE, where it is multiplied by the U subcarrier from the Output Timing card (via the registers AE and BF, and EE and CF). The U Chrominance produced is clocked through the registers CE and HF into the adder circuit KE, IF and JF. This adds the U and V Chrominance data to produce composite Chrominance.

(d) V MODULATOR

The output from the V blanking proms GC and HC is clocked through the registers ED and EF into the multiplier DE, where it is multiplied by the V subcarrier from the Output Timing card (via the registers BE and BF, and CE and CF). The V Chrominance produced is clocked through the registers FD and HF into the adder circuit KE, IF and JF.

The composite Chrominance from this adder is clocked through the registers NF and LE into the Chrominance DAC OF.

(e) COMPUTER BUS DECODE

The bottom 8 bits of the computer Bus, and the control strobes are decoded by the PAL CA to produce the appropriate clocks and enables for the computer loaded registers on this card.

4:4:3 Presets

(a) VR1: Not used

(b) VR2: Chrominance amplitude

(c) VR3: Luminance amplitude

FIGURE 4.4.1 17655C CODER BLOCK DIAGRAM

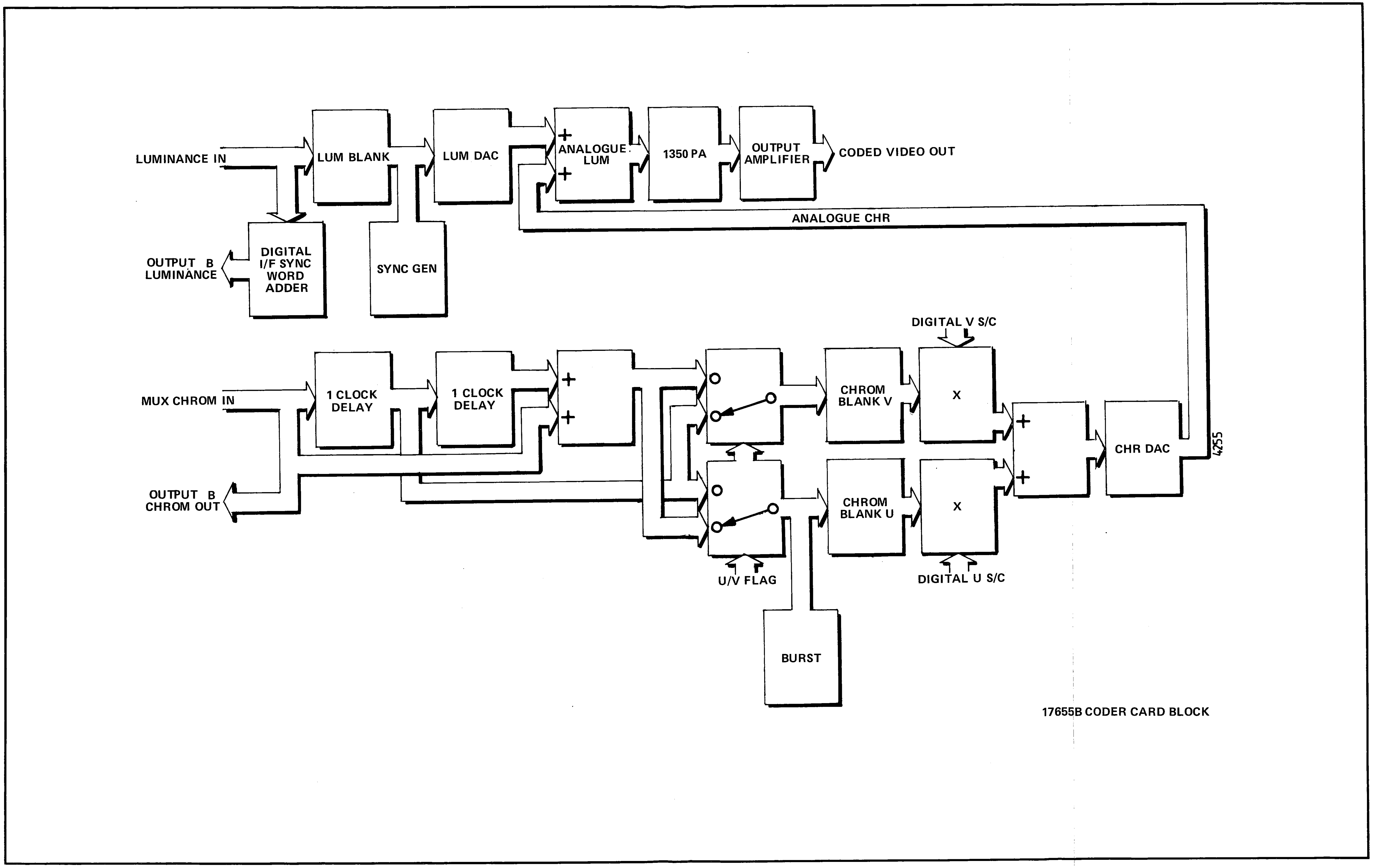
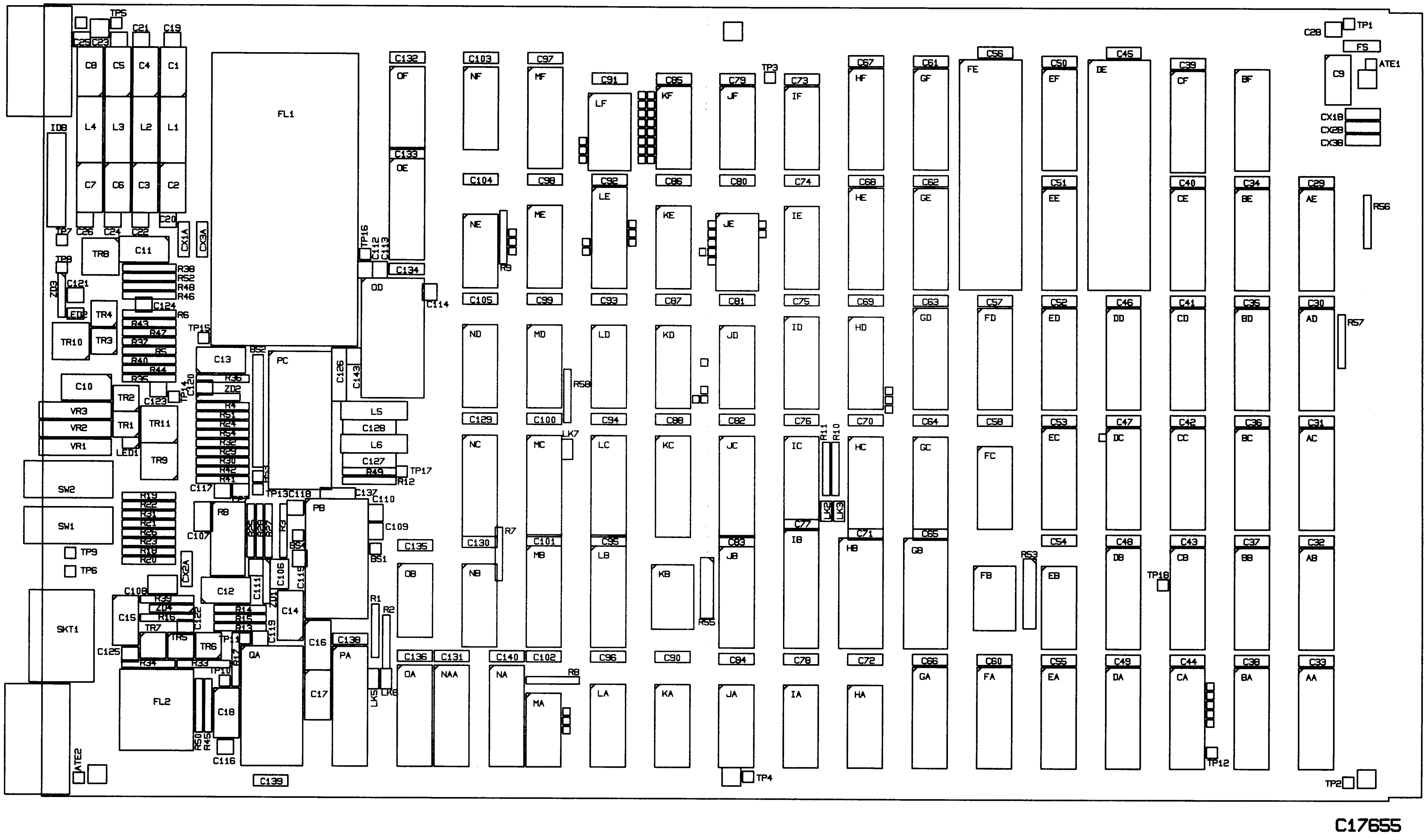
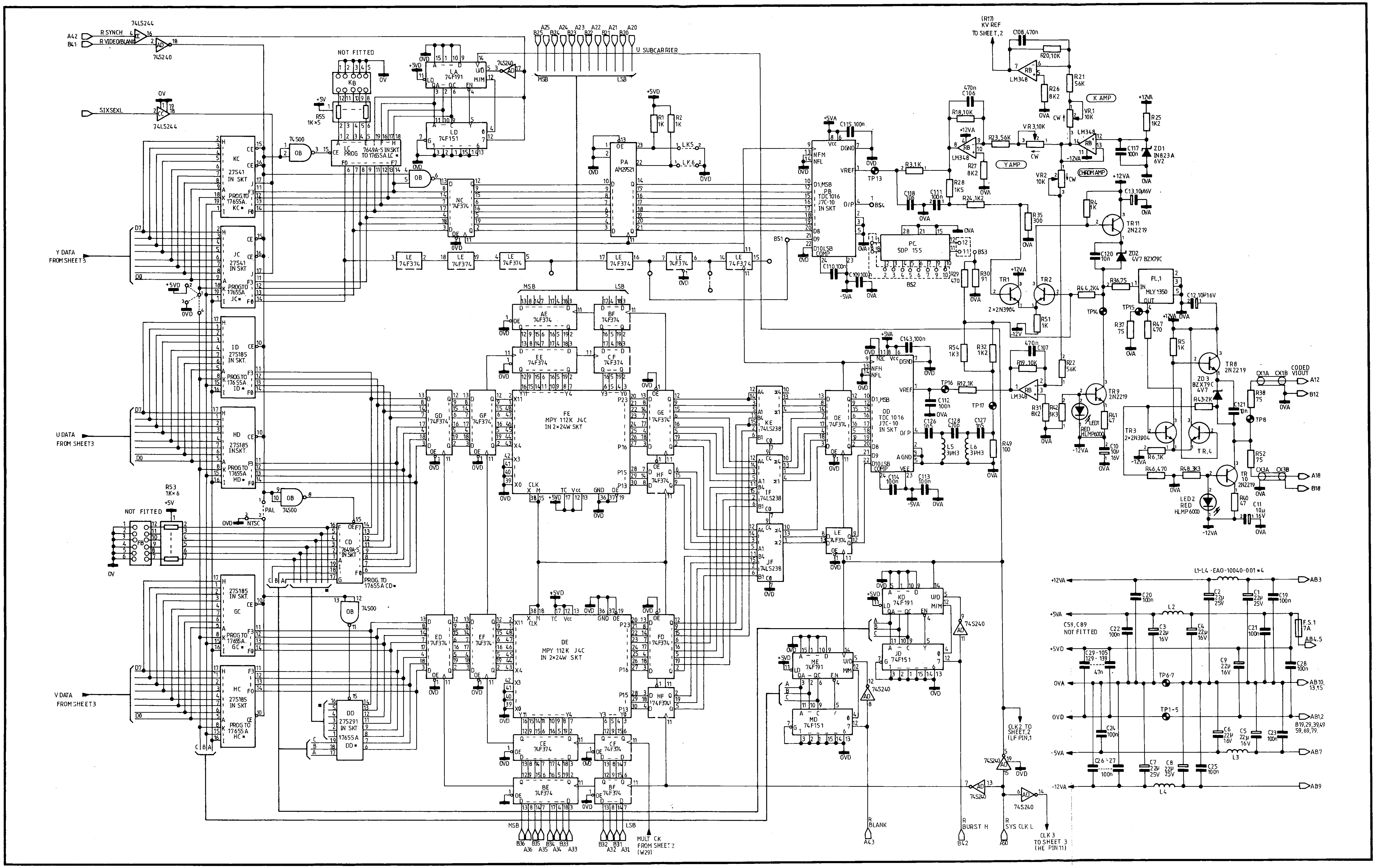


FIGURE 4.4.2 17655C CODER LAYOUT



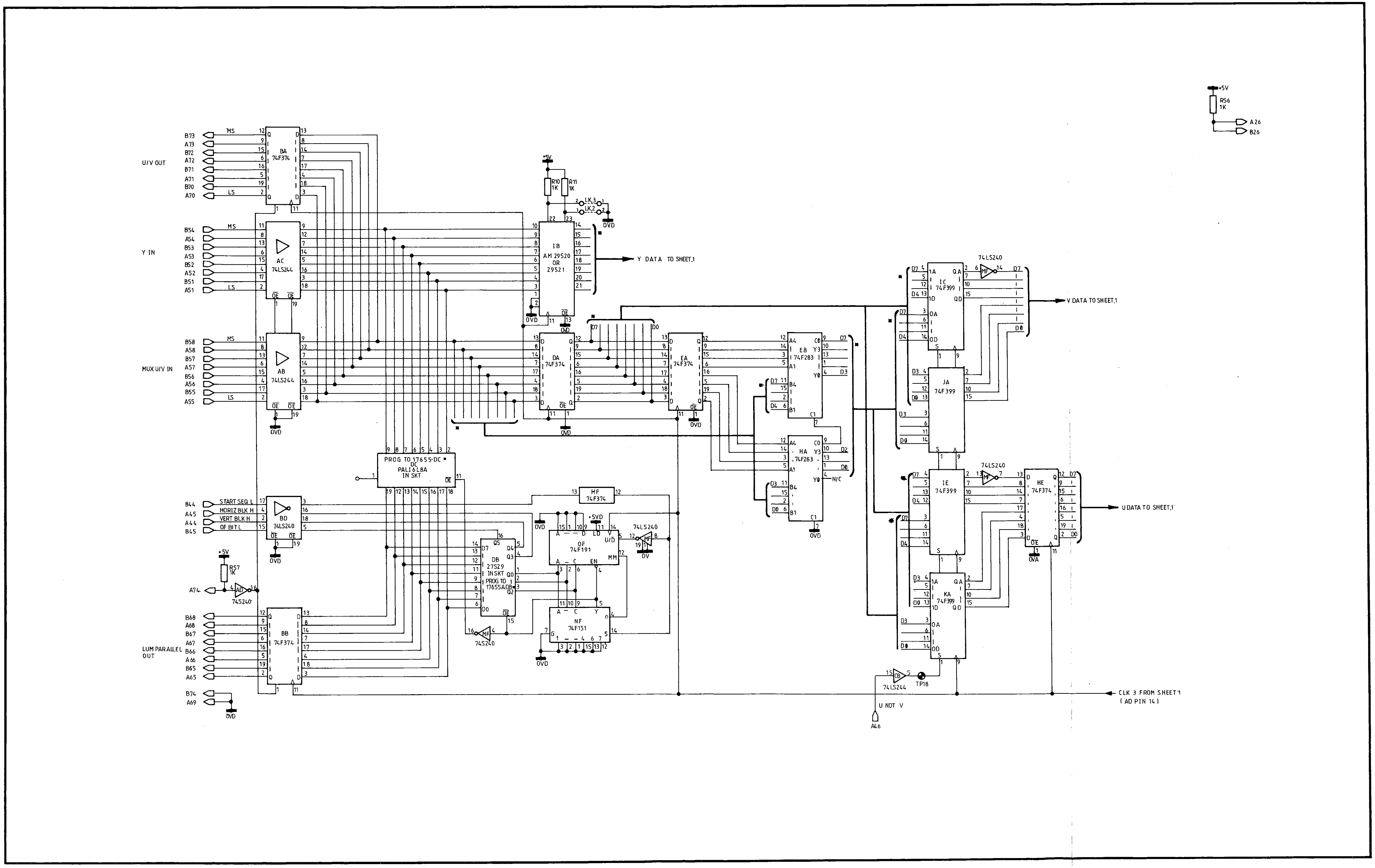
(4,4C)

FIGURE 4.4.3 17655C CODER CIRCUIT 1



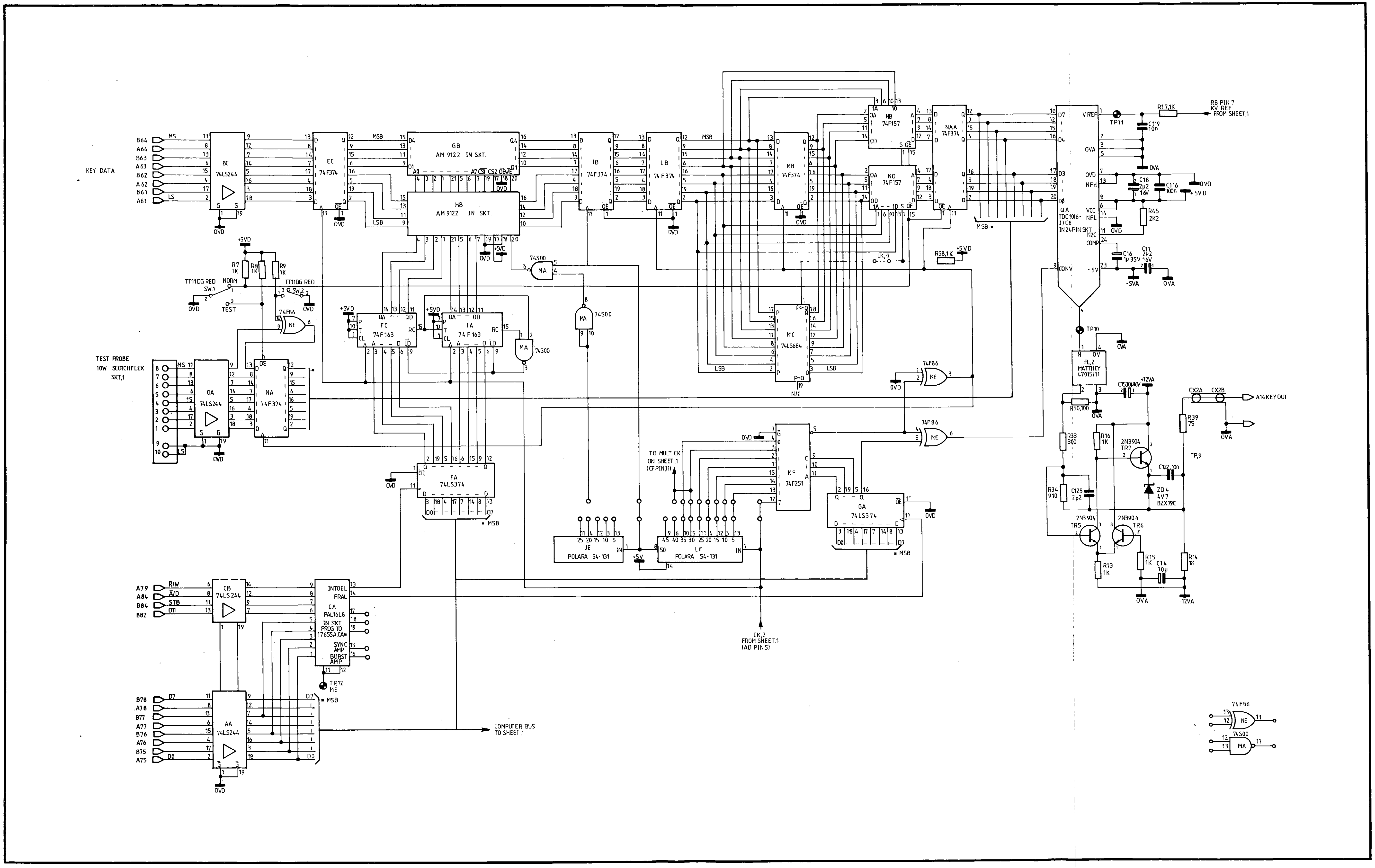
(4,4C)

FIGURE 4.4.4 17655C CODER CIRCUIT 2



(4,4C)

FIGURE 4.4.5 17655C CODER CIRCUIT 3



PAL CHROMA PROCESSOR CARD 17656B

4:5:1 Function

This card in conjunction with the ADC card forms the "adaptive Comb Filter" and decoder of the system. This provides wide-band Combed Luminance, and demodulated U and V components.

The Chroma Proc card accepts Middle-LF Luminance (1H delayed), and Early, Middle and Late-HF Luminance + Chrominance data, from the ADC card, to produce Combed Chrominance and Luminance.

The Input Timing card provides data used to produce digital U and V subcarriers; used to demodulate the Combed Chrominance data.

The Chroma Proc card uses the following methods to produce correctly Combed Chrominance and Luminance data:

HF Luminance:

Early (HF+CHR) + Late (HF+CHR)

Combed Chrominance:

Middle (HF+CHR) - HF Luminance

Combed Luminance:

Middle LF Luminance + HF Luminance

"Comb Fail":

Early (HF+CHR) - Late (HF+CHR)

When "Comb Fail" occurs the Chrominance output of the Comb becomes the Middle HF+CHR data, and the Combed Luminance becomes Middle LF Luminance.

4:5:2 Circuit Description

(a) HF LUMINANCE DATA PATH

Late HF+CHR data is buffered by AD and clocked through the registers BD and CD into the Phase advance circuit; consisting of the proms DD and CC, the registers ED and DC, and the adder circuit FD and FC.

(4,5B)

Early HF+CHR data is buffered by AB and clocked through the registers BB, CB and DB into the phase delay circuit; consisting of the proms EB and DE, the registers FB and EE, and the adder circuit GE and GD.

The phase advanced Late HF+CHR data is passed to the adder circuit HD, HC and GC, where phase delayed Early HF+CHR is added. The output of this adder is Combed HF Luminance.

(b) COMBED CHROMINANCE PATH

The HF Luminance data from the output of the adder HD, HC and GC, is inverted and delayed by IB, and added to the Middle HF+CHR data (buffered by AC and delayed by the pipe line register BC) in the adder circuit HE and IC. This produces Combed Chrominance data at the output of the pipe line register IE.

(c) COMBED LUMINANCE PATH

The HF Luminance data produced by the adder circuit HD, HC and GC is clocked through the pipe line register GB into the scaling prom HB. This scaled HF Luminance data is clocked through the register GA into the adder CG, DG and EG, where LF Luminance from CE (buffered by AE and clocked through the registers BE and CE) is added. The output of the adder CG, DG and EG is wide-band Combed Luminance data.

The wide-band Luminance data is range-limited by the selectors CH and DH, and then clocked through the pipe line registers EH, FH and AM, then passed to the Input Switch card.

(d) COMB FAIL CIRCUIT

Early and Late HF+CHR data from BB and BD, are rectified in the proms CA and EC then added by CF and DF. The output of this adder is clocked through the register FF into the thresh-hold level prom FE, which provides the Comb Fail flag. This flag is stretched by FN and IN to produce a disable signal, which turns off the HF Luminance at IB and GA. This produces Middle HF+CHR at IE, and Middle LF Luminance at FH.

The Comb Fail flag also turns off the "Post Demodulator Comb" circuit when the Comb fails; putting the decoder into simple operation.

(e) CHROMINANCE DEMODULATORS

Chrominance data from IE is passed to the multipliers HH and HF, where it is demodulated by the U and V subcarriers; generated by the proms HL, HM and HN (for U), and HI, HF and HK (for V). These proms are supplied with a rotational picture point count provided by the Input Timing card; buffered by BI and AI and registered by CI and EI.

(f) POST DEMODULATOR COMBS

The U and V base band components produce by the multipliers HF and HH are clocked through the pipe line registers GG and GH into the Rams GN, GM, CL, CK, GJ and GT. These Rams produce a 1H delay; achieved by addressing the Rams with a repeating picture point count from FI, EJ and GF, and by clocking the stored data out before writing new data in. The Read clocks and Write enable signals for the Rams are provided by the delay lines EN and EM, with associated circuitry.

The 1H delayed U and V are clocked through the registers FM and FL in conjunction with the undelayed U and V from FJ and FK, into the adder circuits EL, CJ and DJ (for U), and CK, DK and EK (for V). The Combed U and V components produced are clocked through the registers AJ and BK, and then passed to the Chroma Filter card.

The registers BJ and AK provide the U and V bypass paths, when Comb Fail occurs.

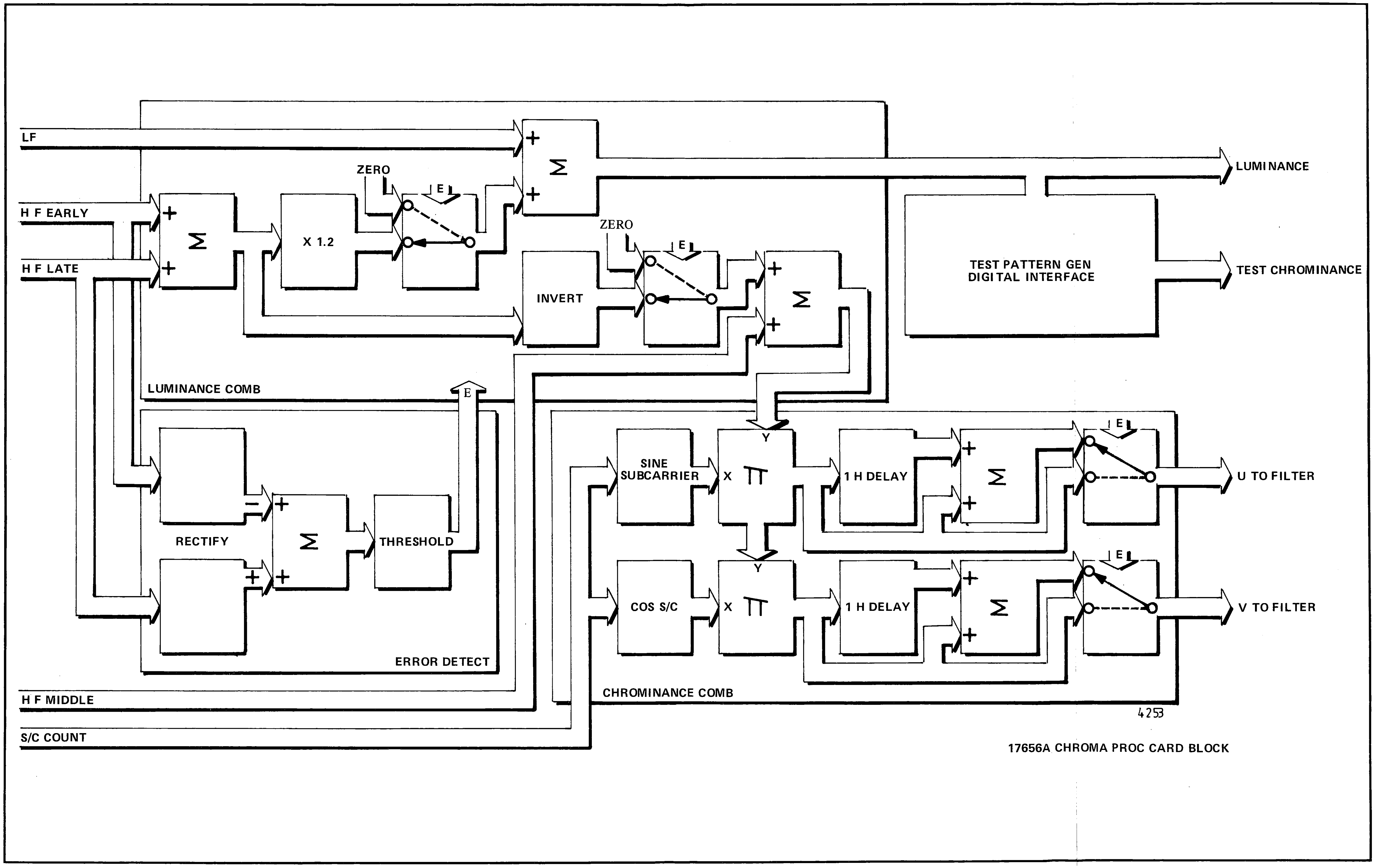
(g) DIGITAL INTERFACE CIRCUIT

Luminance and U/V data from the "INPUT B" connector, are buffered by AH and AG , then clocked through the registers BH and BM, and BG and BL. These output when enabled by the computer bus decode circuit, and the PAL CM subsequently decodes the data sync word from the luminance data. This provides the appropriate timing signals required by the Input Timing card when Digital input video is selected.

(h) COMPUTER BUS DECODE

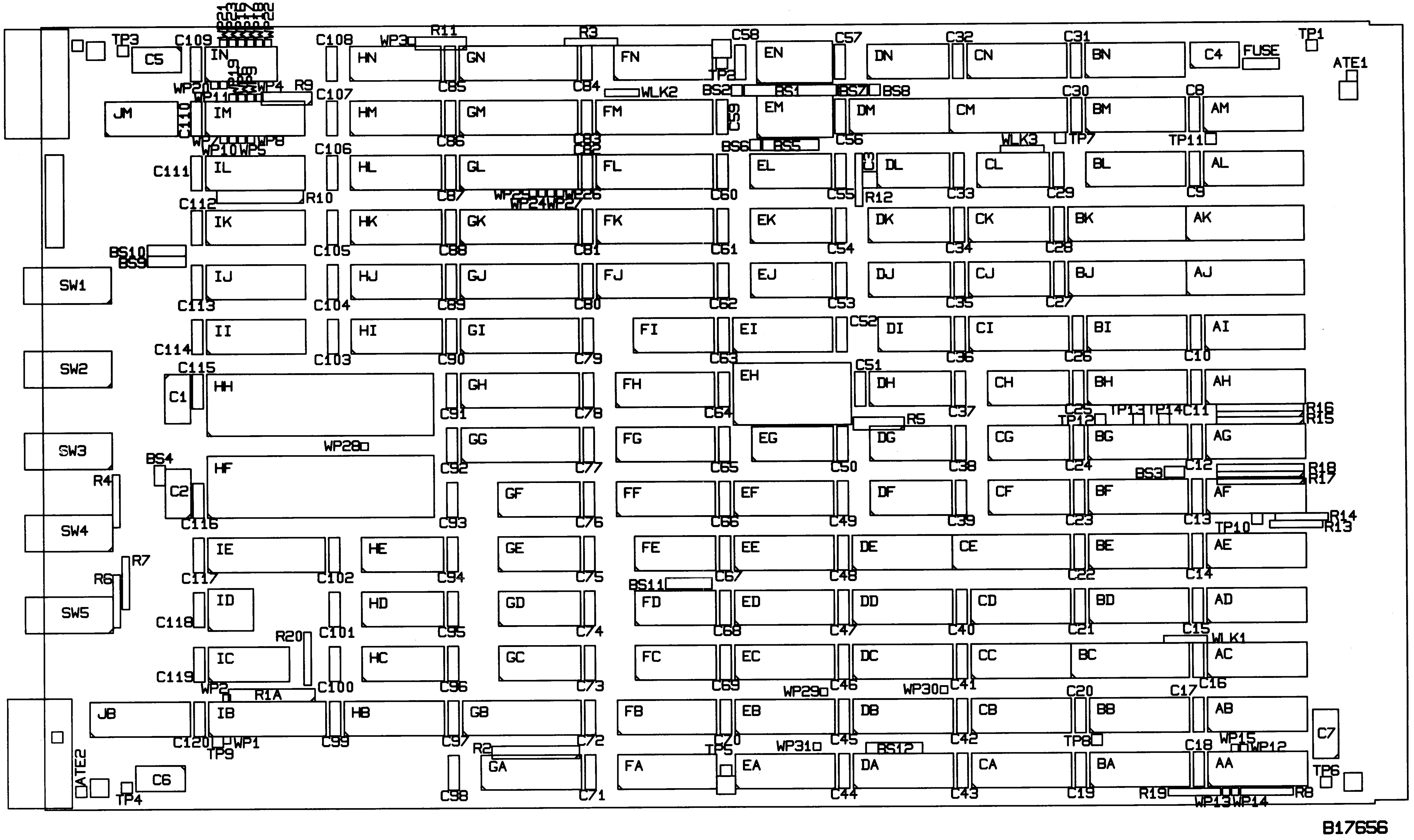
The system computer bus is buffered by BA and AA then passed to the bus decoder-PALs EF and DA, which provide the necessary enables for the computer controlled circuitry on this card.

(4,5B)
FIGURE 4.5.1 17656B CHROMA PROC BLOCK



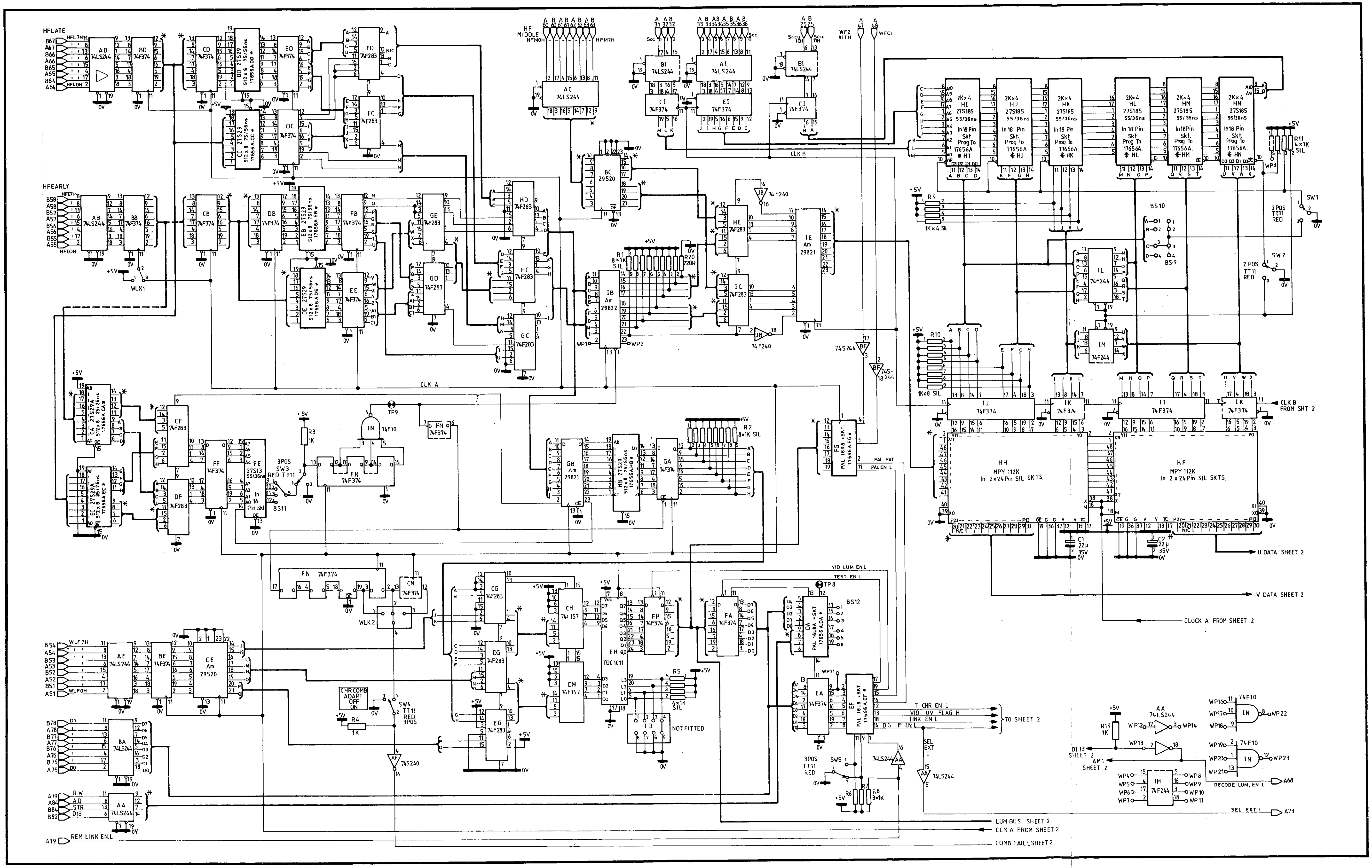
(4,5B)

FIGURE 4.5.2 17656B CHROMA PROC LAYOUT



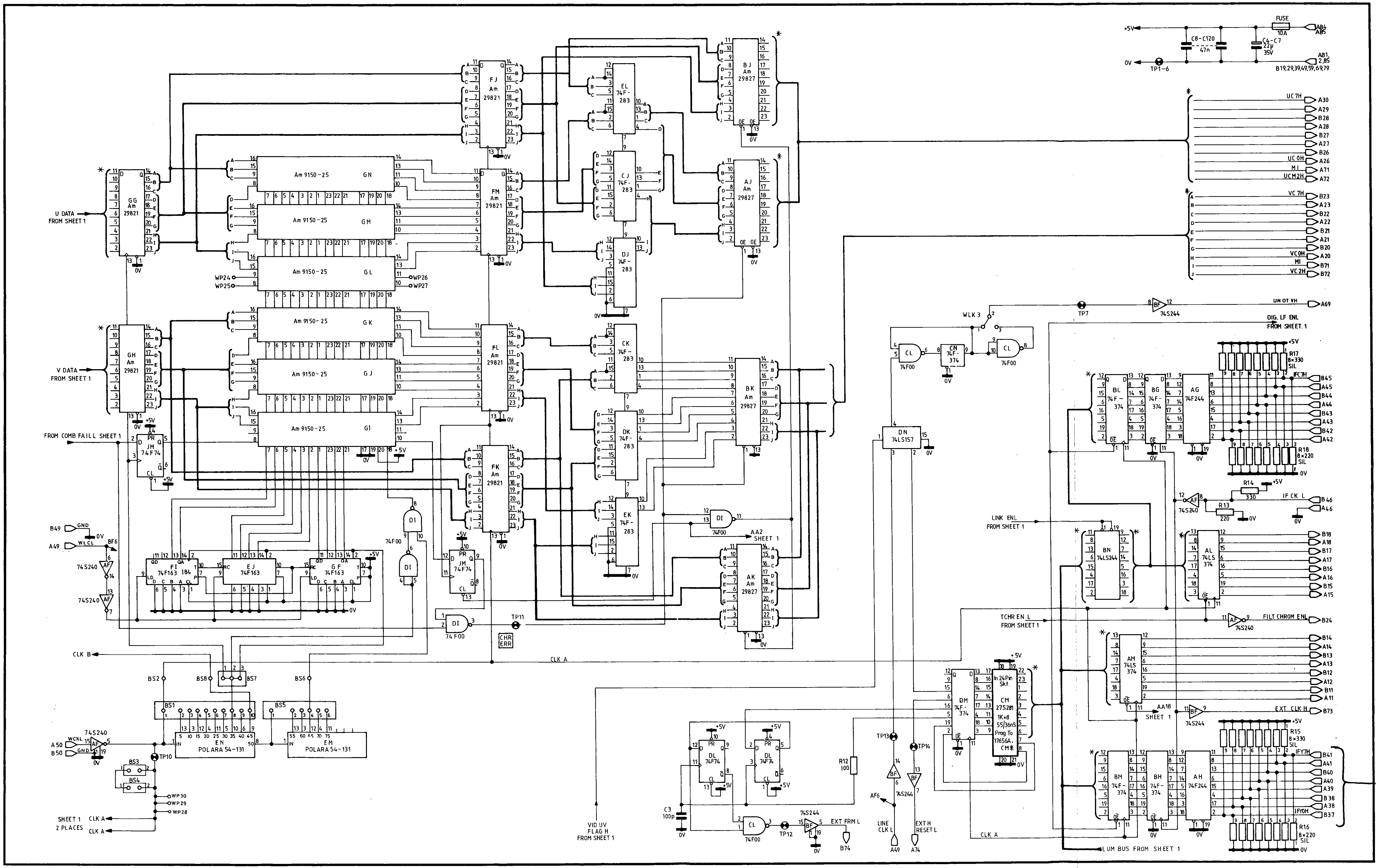
(4,5B)

FIGURE 4.5.3 17656B CHROMA PROC CIRCUIT 1



(4,5B)

FIGURE 4.5.4 17656B CHROMA PROC CIRCUIT 2



INPUT B.
(ENCORE)
VIA
I/O EXPANDER

PAL FILTER CARD 17657C

4:6:1 Function

The function of this card is to remove any unwanted frequency components, from the U and V base band data, produced by the demodulation process carried out on the Chroma Processor card.

The card consists of two identical 9-Tap Finite Impulse Response filter circuits; one for U and one for V.

The filter U and V data produced, is range-limited, multiplexed together and then passed to the Input Switch card.

4:6:2 Circuit Description U Data Path

(a) FILTER TAPS 1 AND 9

U data from the Chroma Processor card is buffered by AC and clocked through the registers KH, KJ, KK, KL, JK, JJ and JI, which form the Taps 1 to 9 of the filter.

Tap 1 data from KH and Tap 9 data from JI are added by KG, JH and JG, and clocked through the register GG into the scaling proms FG and GH. These proms scale the data to produce -0.005 of the data. The scaled data is clocked through the registers EG and EH into the second level adder circuit DG, DI and DH.

(b) FILTER TAPS 2 AND 8

Tap 2 data from KI and Tap 8 data from JJ are added by IH, II and HI, and clocked through the register GI into the scaling proms FI and FH. The data produced is clocked through the registers EI and EH into the second level adder circuit DG, DI and DH.

The output of the adder DG, DI and DH is passed to the third level adder circuit CH, CI, CJ and CK, where scaled data from the second level adder DJ, DL and DK is added.

(c) FILTER TAPS 3 AND 7

Tap 3 data from KJ and Tap 7 data from JK are added by HK, IJ and HJ, and clocked through the register GJ into the scaling proms FJ and GK. The data produced is clocked through the registers EJ and EK into the second level adder circuit DJ, DL and DK.

(d) FILTER TAPS 4 AND 6

Tap 4 data from KK and Tap 6 data from JL are added by IL, HL and IK, and clocked through the register GL into the scaling proms FL and FK. The data produced is clocked through the registers EL and EK into the second level adder circuit DJ, DL and DK.

The output from the adder DJ, DL and DK is passed to the third level adder circuit CH, CI, CJ and CK. The output of this adder is passed to the final level adder circuit BH, BI, BJ and BK.

(e) FILTER MIDDLE TAP

Middle Tap data from JK is scaled by the proms HH and HG, to produce 0.34 of the data. This scaled data is clocked through the registers BG and IG into the final level adder circuit BH, BI, BJ and BK.

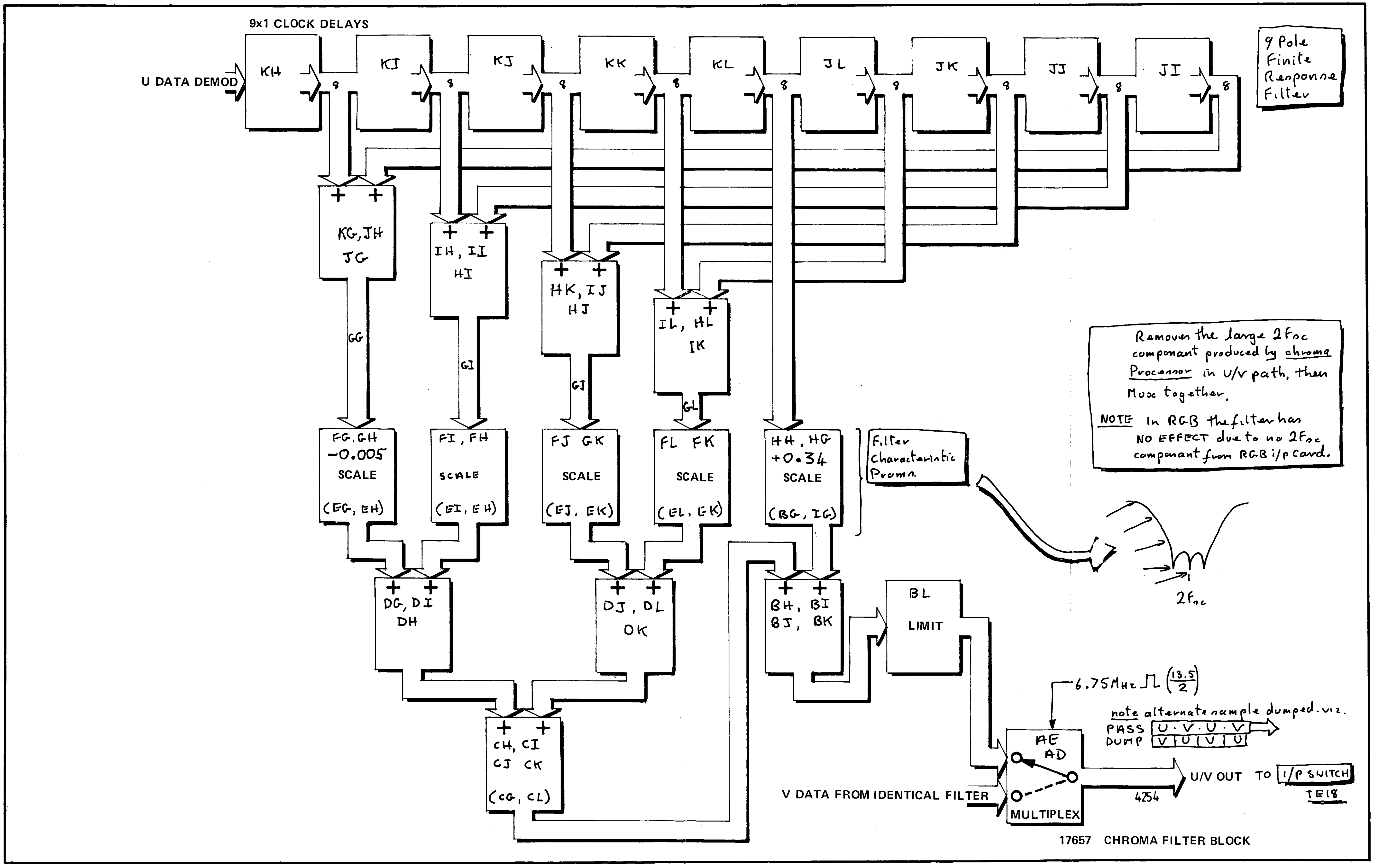
The filtered data produced at the output of the final level adder is range-limited by the PAL BL, and clocked through the registers AE and AD, where the filtered U and V data are multiplexed before being passed to the Input Switch card.

4:6:3 **Fault Location**

Faults can be located by making both filter paths the same, and using the one bit compare probes:

Make U=V using the Chroma Processor card diagnostic switches and then make point to point comparisons using the probes.

FIGURE 4.6.1 17657C CHROMA FILTER BLOCK



Removes the large 2Fsc component produced by chroma Processor in U/V path, then Mux together.

NOTE In RGB the filter has NO EFFECT due to no 2Fsc component from RGB i/p card.

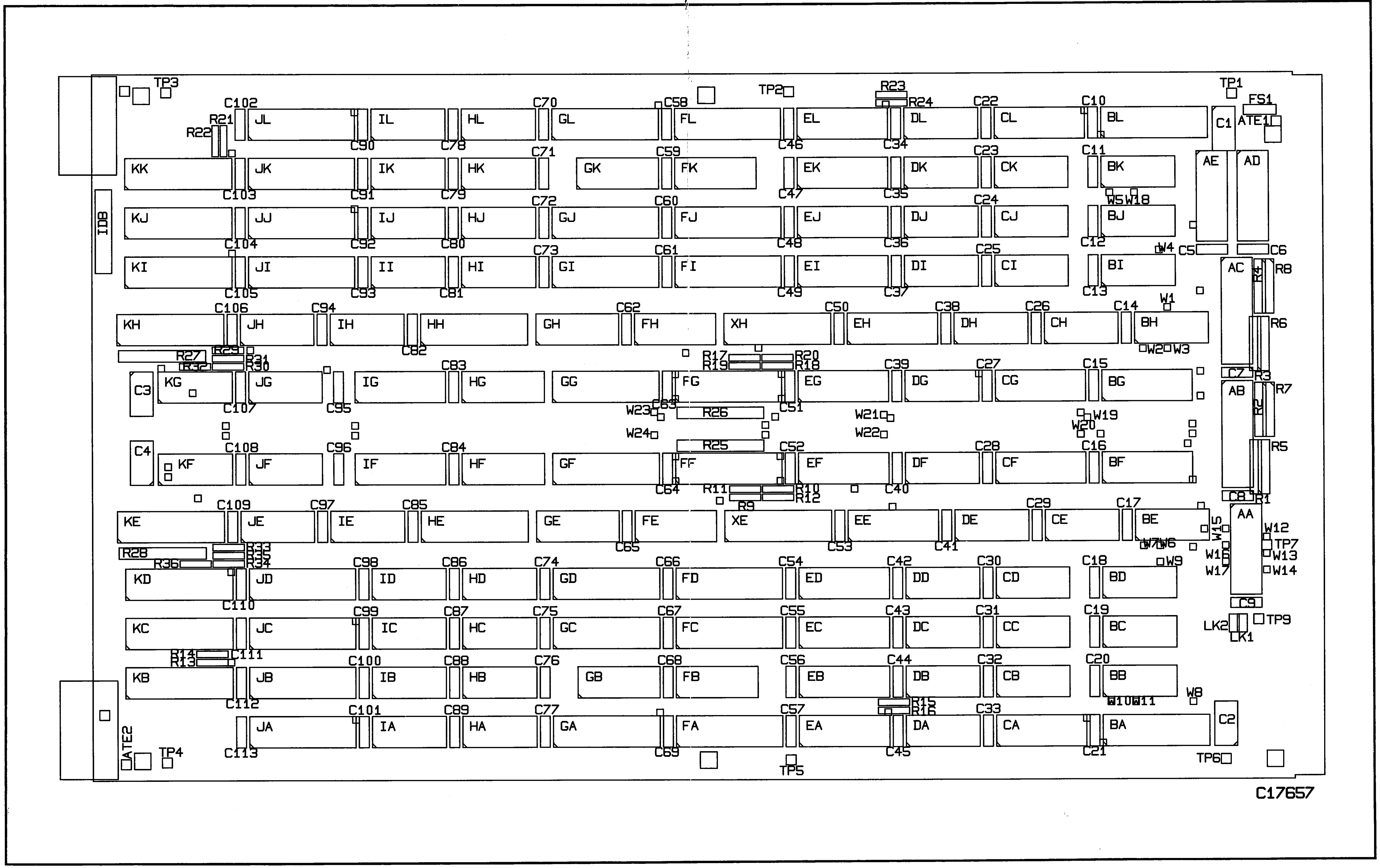
note alternate sample dumped. viz.

PASS U · V · U · V

DUMP V U V U

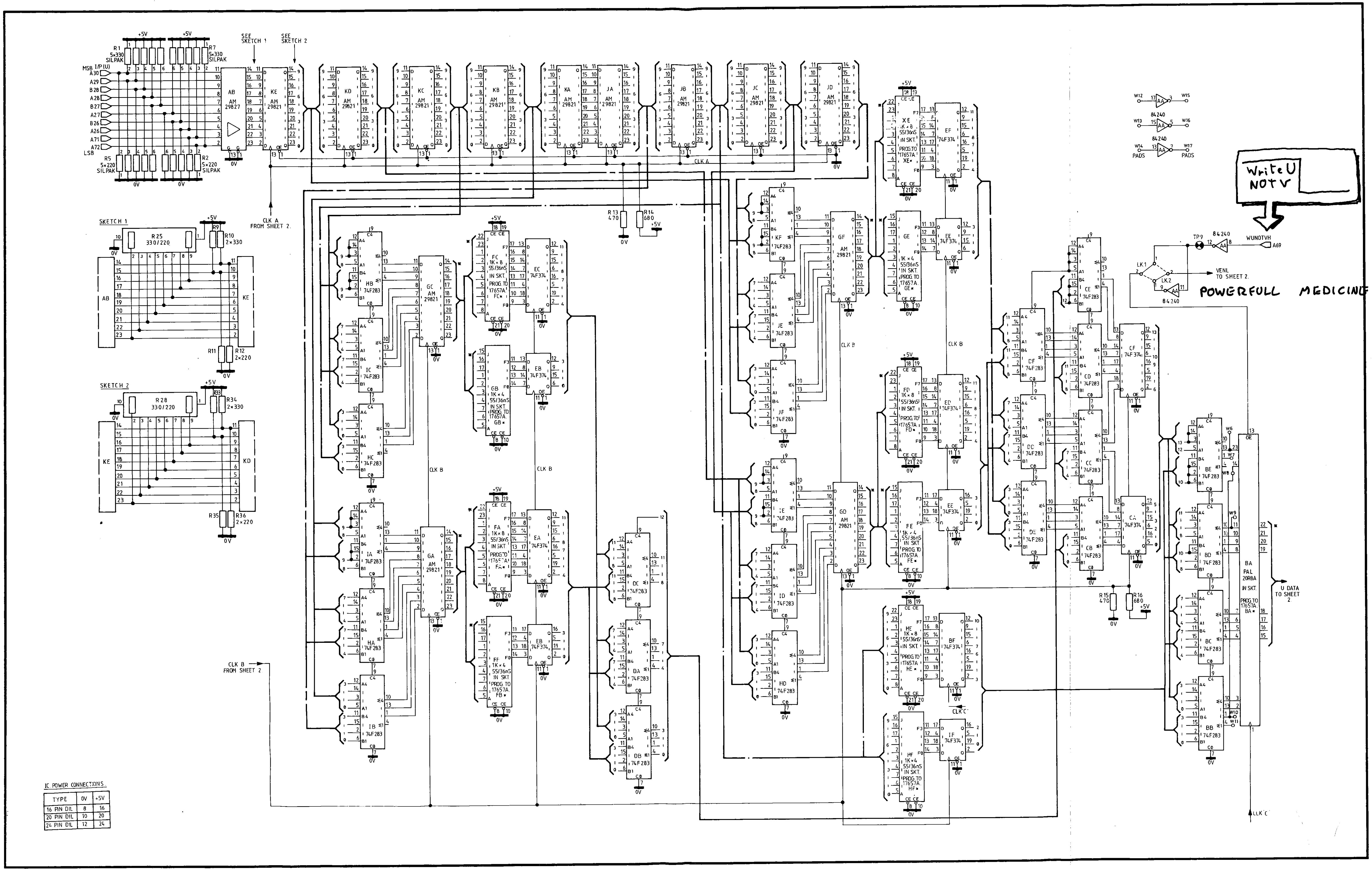
17657 CHROMA FILTER BLOCK

(4,6C)
FIGURE 4.6.2 17657C CHROMA FILTER LAYOUT



(4,6C)

FIGURE 4.6.3 17657C CHROMA FILTER CIRCUIT 1



Write U NOT V

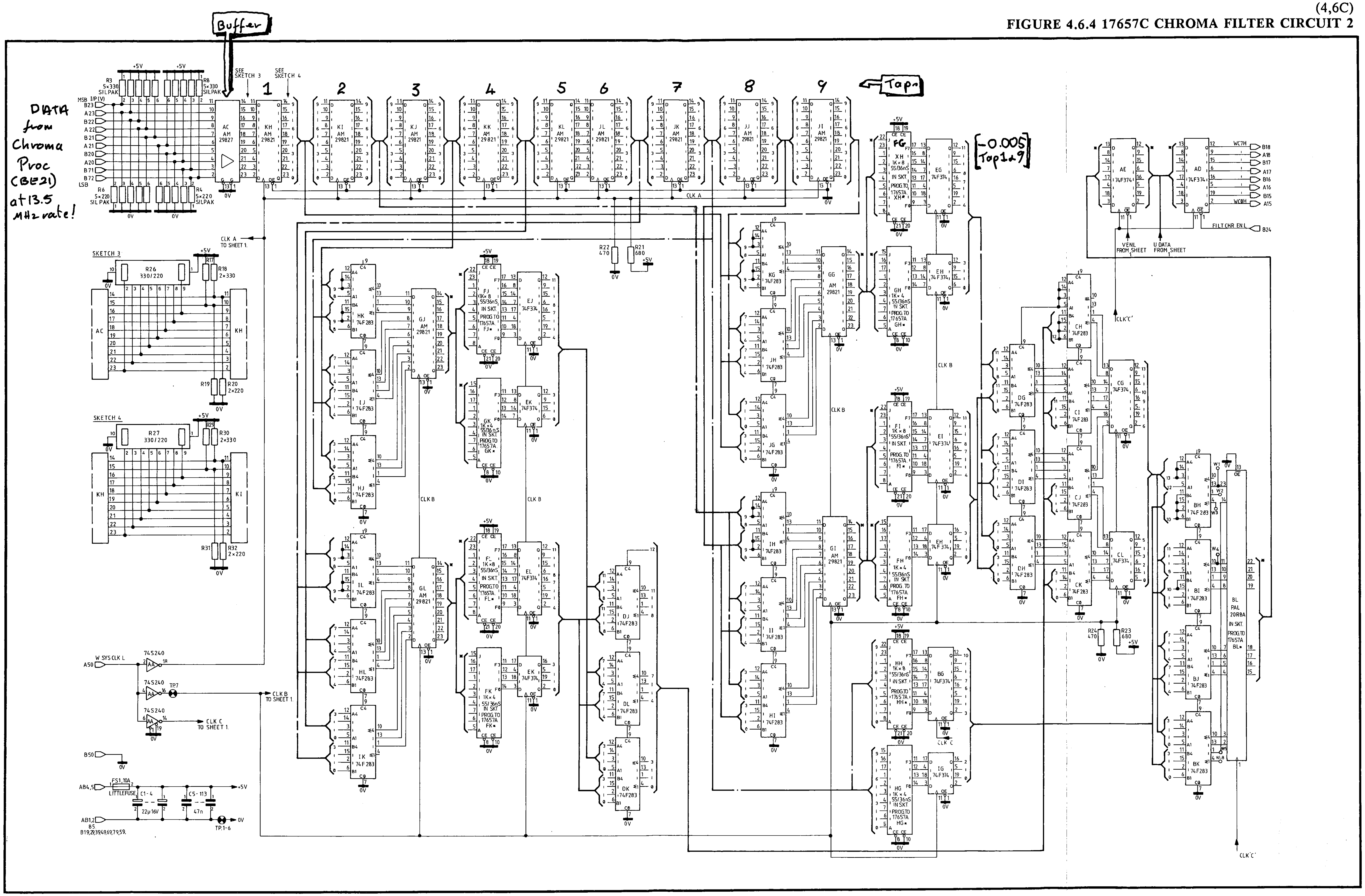
POWERFULL MEDICINE!!!

IC POWER CONNECTIONS.

TYPE	0V	+5V
16 PIN DIL	8	16
20 PIN DIL	10	20
24 PIN DIL	12	24

(4,6C)

FIGURE 4.6.4 17657C CHROMA FILTER CIRCUIT 2



NTSC FILTER CARD 17673B

4:7:1 Function

The function of this card is to remove any unwanted frequency components, from the U and V base band data, produced by the demodulation process carried out on the Chroma Processor card.

The card consists of two identical 5-Tap Finite Impulse Response filter circuits; one for U and one for V.

The filtered U and V data produced, is range-limited, multiplexed together and the passed to the Input Switch card.

4:7:2 Circuit Description U Data Path

(a) FILTER TAPS 1 AND 5

The U data from the Chroma Processor card is clocked through the registers AE, BE, CE, DE and EE, which form the Taps 1 to 5 of the filter.

Tap 1 data from AE and Tap 5 data from EE are added by the adder circuit AC, AB and AA, and clocked through the register BB into the scaling proms BA and CA. The data produced is clocked through the registers CB and CC into the second level adder circuit DA, DB and DC.

(b) FILTER TAPS 2 AND 44

Tap 2 data from CE and Tap 4 data from EE are added by the adder circuit CD, BD and BC, and clocked through the register DD into the second level adder circuit DA, DB and DC. The output from this adder is passed to the final adder circuit EA, EB and EC.

(c) FILTER MIDDLE TAP

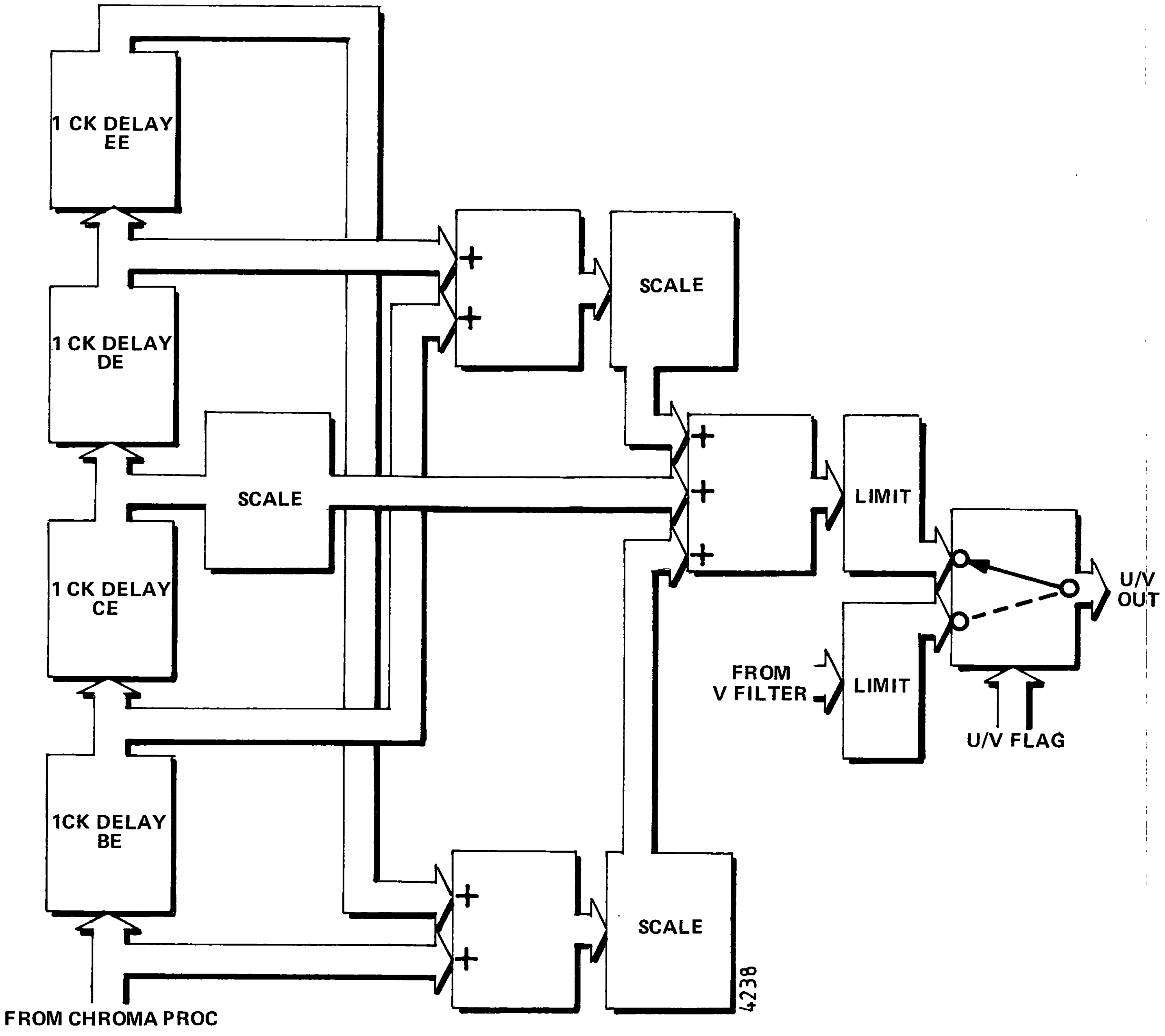
Middle Tap data from DE is scaled by the proms FE and FD. This scaled data is clocked through the registers GE and GD into the final adder circuit EA, EB and EC. The filtered U data produced by this adder is clocked through the registers GD and FA into the range-limiter circuit FB, FC and ED, which also forms the U/V multiplexer circuit. The U/V data is clocked through the register AG and passed to the Input Switch card.

4:7:3 Fault Location

Faults can be located by making both filter paths the same, and using the one bit compare probes on the top MUX/DEMUX card.

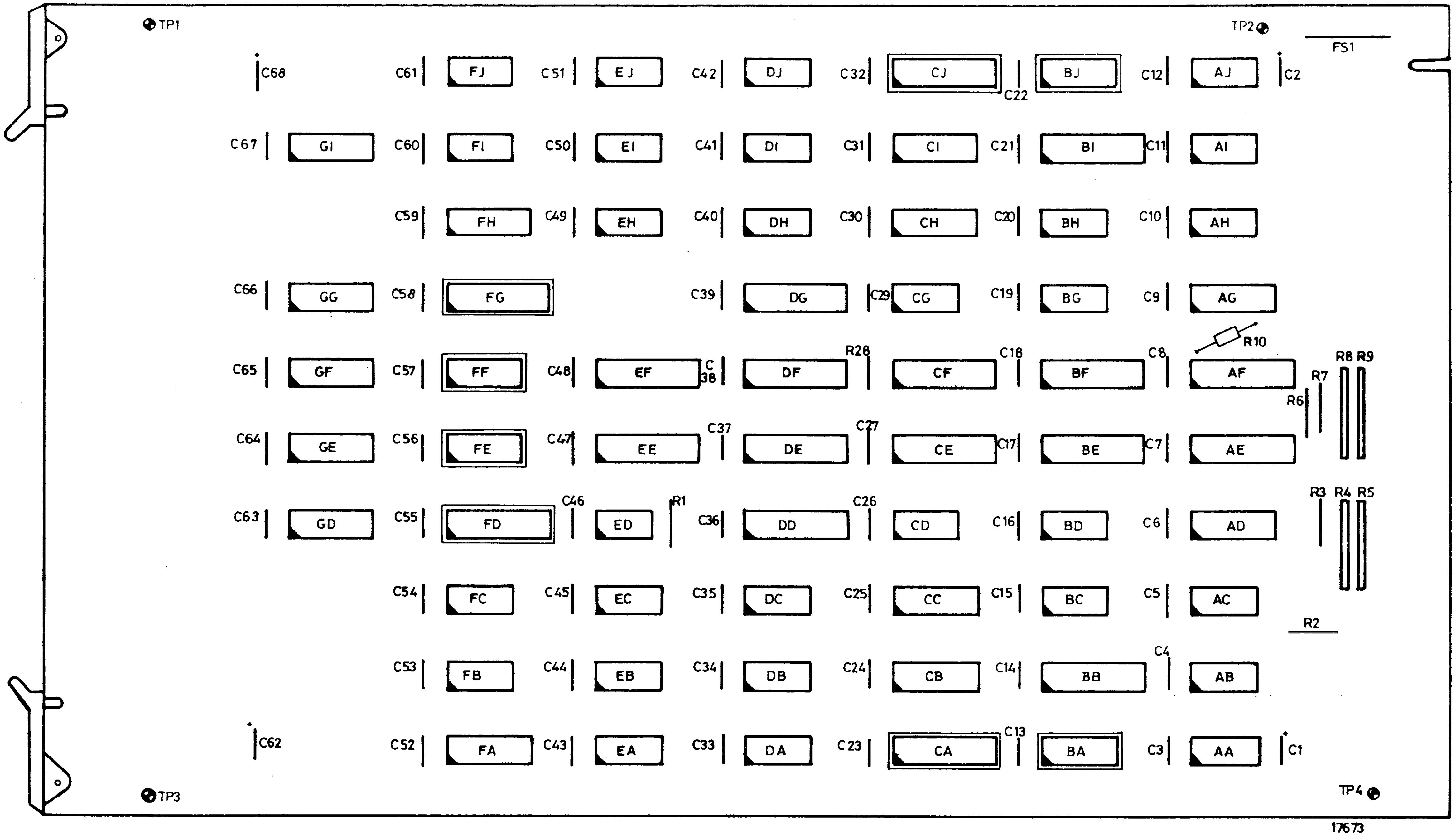
Make U=V using the Chroma Processor card diagnostic switches and then make point to point comparisons using the probes.

FIGURE 4.7.1 17673B CHROMA FILTER BLOCK



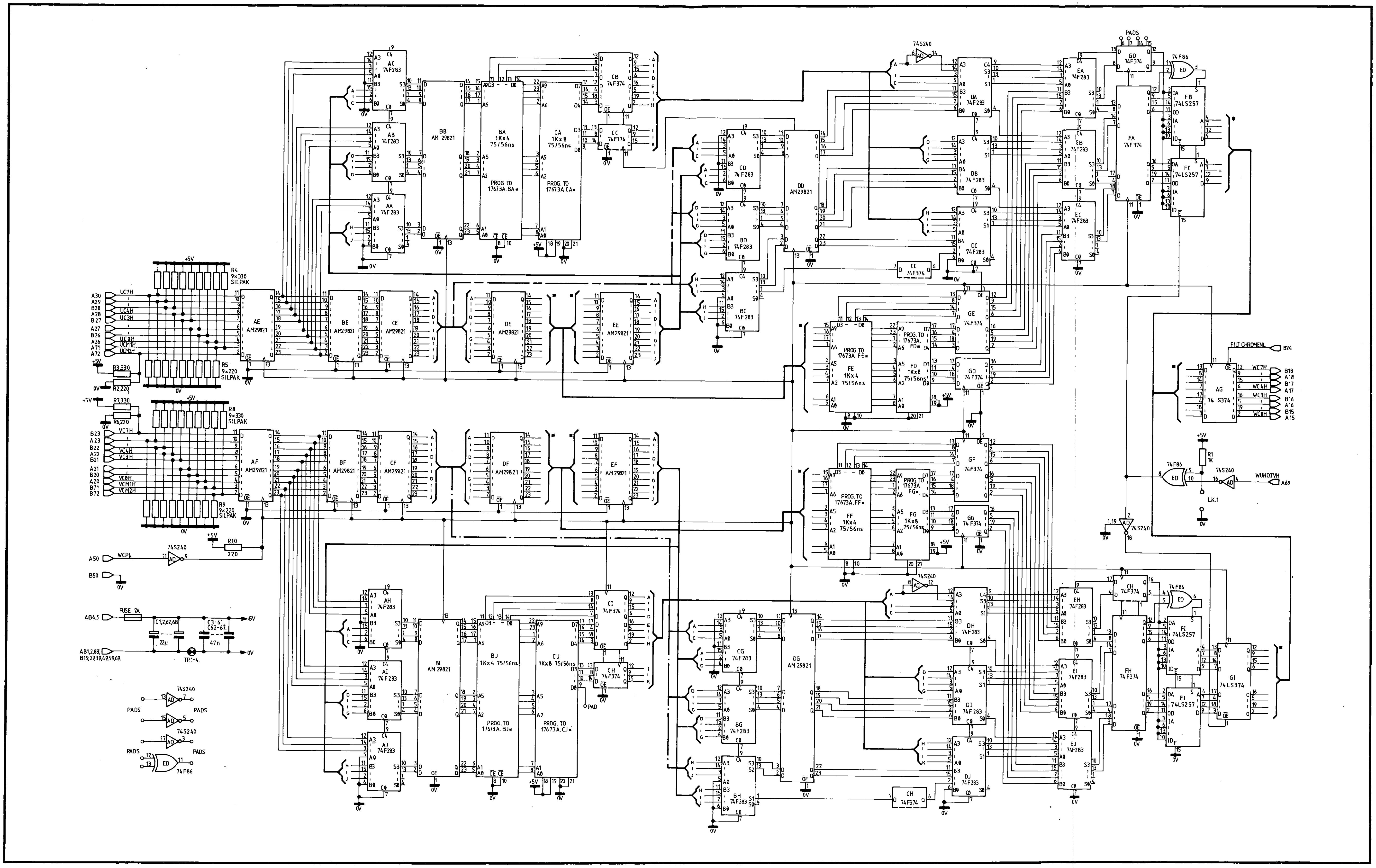
17673B CHROMA FILTER CARD BLOCK

(4,7B)
FIGURE 4.7.2 17673B CHROMA FILTER LAYOUT



(4,7B)

FIGURE 4.7.3 17673B CHROMA FILTER CIRCUIT



ADC CARD 17676D

4:8:1 Function

The main function of this card is to buffer, black level clamp then separate the input Coded video signal into LF Luminance, and HF Luminance plus Chrominance data, required by the Chroma Processor card to Comb filter and decode the coded video.

This card also provides digital coded test videos which can be used to prove the operation of various cards in the system.

4:8:2 Circuit Description

(a) ANALOGUE CODED VIDEO PATH

Coded input video is Buffered by TR 29, PF and associated components then amplified by OF. The complimentary current output from OF is amplified and then converted back to voltage form by the discrete amplifier circuit consisting of TR4, TR5, TR7, TR16, TR27 and TR28. The output from this amplifier is passed to PE which drives the Luminance signal into the Delay lines QD, PD, OD and MD.

(b) ANALOGUE LF LUMINANCE PATH

Luminance from PE (TP6) is amplified by the current amplifier circuit ME, TR25 and TR26, then passed to LE (TP14) which drives the Luminance into the Low Pass filter FL2. The output from this filter (TP16) is buffered by JE into the black level sampler (TP12) circuit IE, LD and TR4, and the ADC IF via the discrete filter circuit, and the buffer JF (TP13).

(c) ANALOGUE HF LUMINANCE + CHROMINANCE PATH

LF Luminance from FL2 (TP16) is subtracted from the filtered Coded video from the output of FL1 (TP15) to produce HF Luminance plus Chrominance at the input of KD (TP11). The buffered HF is passed to the ADC ID via the discrete filter circuit, and the buffer JD (TP10).

(d) BLACK LEVEL CLAMP

LF Luminance (TP12) is sampled by IE, and the sample voltage is buffered by LD and passed to the offset and filtering circuit LD and associated components. The black level compensating offset produced is passed to the amplifier circuit ME, TR25 and TR26, where the offset is added.

(4,8D)

(e) GAIN & OFFSET CONTROL

The Zener Diode ZD4 provides a reference voltage that is used by OP Amps JA and JB, to produces the appropriate Offset and Gain voltages for the ADCs ID and IF, and the clamp circuit. These Gains and Offset voltages are remotely control by the engineering values.

The system bus is decoded by the PAL CA, which controls the DAC HA. This DAC provides the analogue Gain and Offset voltages.

(f) 1 H DELAY CIRCUITS

The LF luminance data from the ADC IF, and the HF data from the ADC ID is clocked through the registers GF and FC into the RAMs DE and EE (to provide Middle LF), and into the RAMs DC, EC, DB and EB (to provide Middle and Late HF). The delayed LF and HF data is clocked through the registers AD, CC and AB and passed to the Chroma Processor card.

The Counters FF, DF and EF produce a picture point count which addresses the RAMs and the Test Proms FD, GD, ED and DD. The data stored in the RAMs is read prior to new data being written, by the Write enable signals from the Delay line HF.

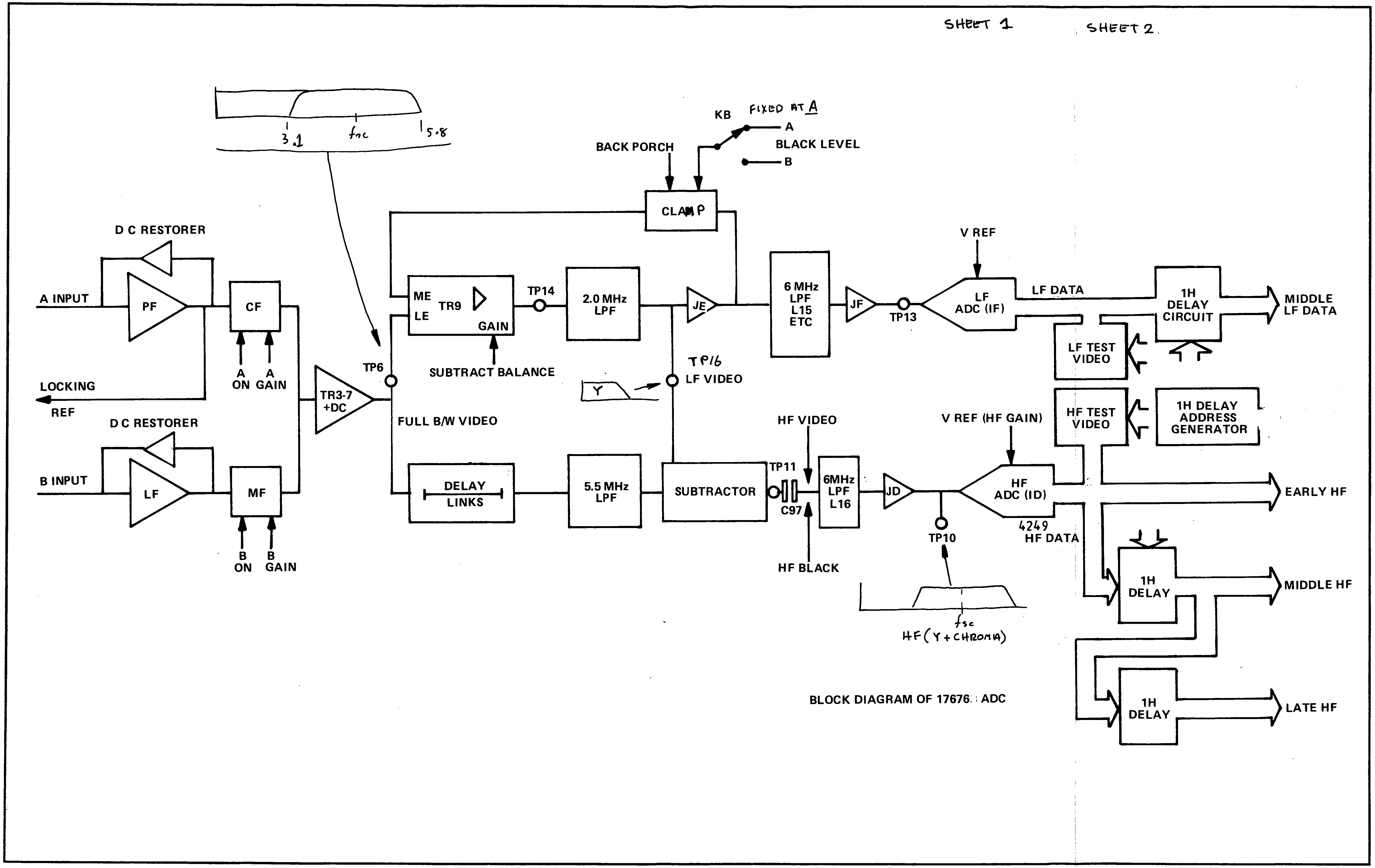
(g) COMPUTER BUS DECODE

The system computer bus is buffered by BA and AA, and decoded by the PAL CA, to provide the enables for the computer controlled circuitry on this card.

4:8:3 Adjustments

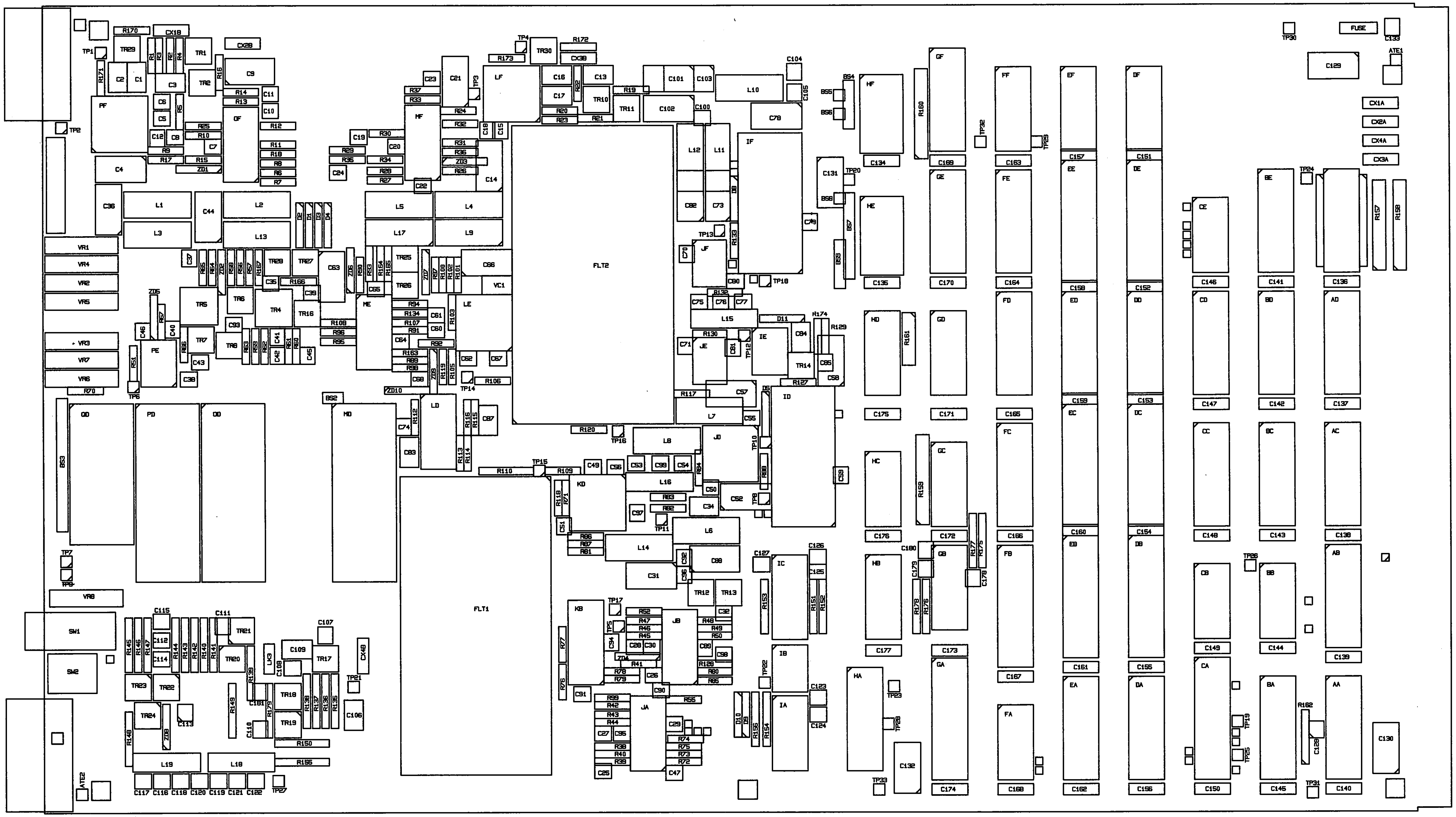
(a)	VR1	Coded input video Gain adjustment
(b)	VR2	Video Gain adjustment (Not used)
(c)	VR3	HF Gain adjustment
(d)	VR4	Coded video black level adjustment
(e)	VR5	Input black level adjustment (Not used)
(f)	VR6	HF offset adjustment
(g)	VR7	HF/LF subtracter balance adjustment

FIGURE 4.8.1 17676D ADC BLOCK



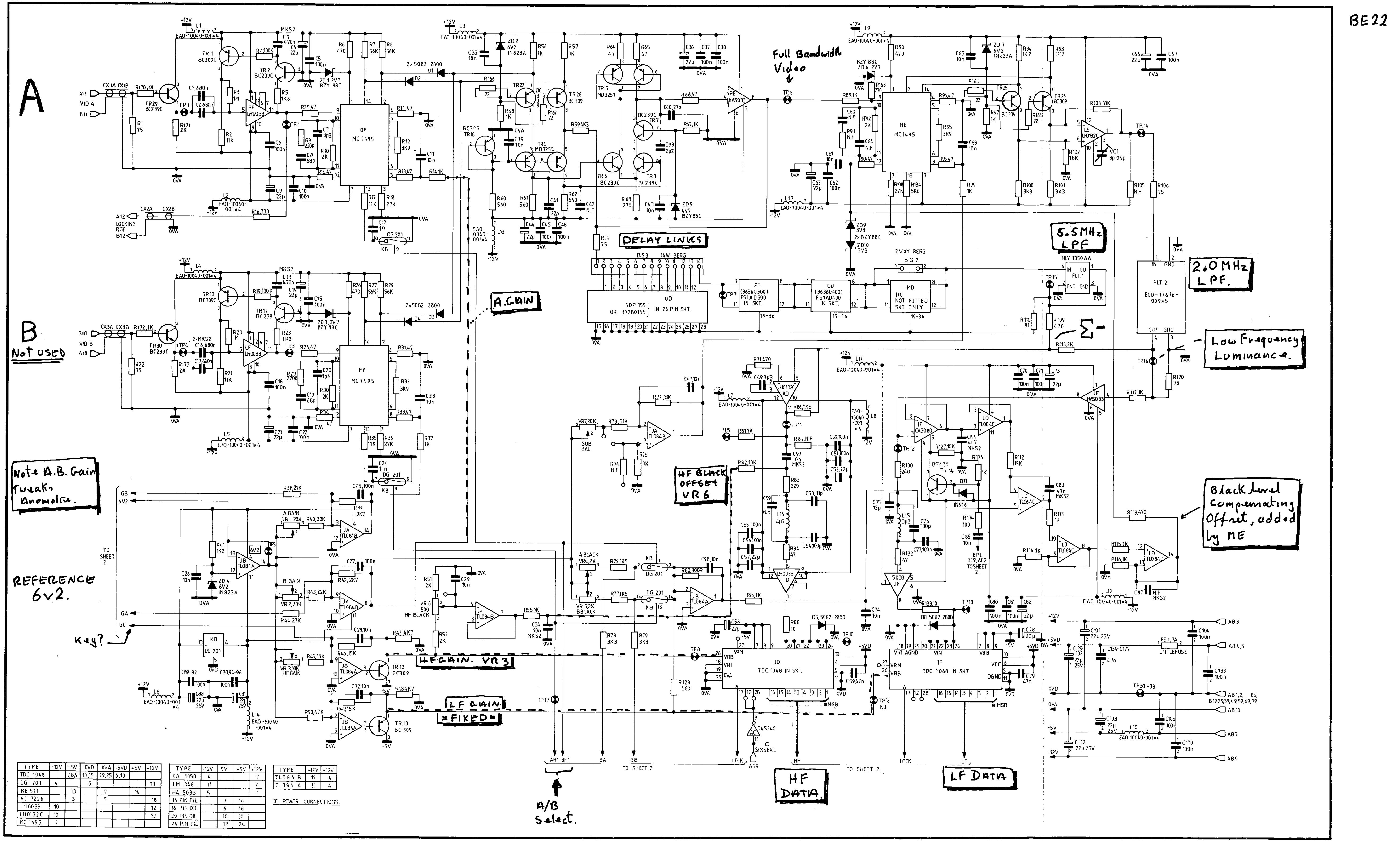
(4,8D)

FIGURE 4.8.2 17676D ADC LAYOUT



(4,8D)

FIGURE 4.8.3 17676D ADC CIRCUIT 1



TYPE	-12V	-5V	0VD	0VA	+5VD	+5V	+12V
TDC 1048		7,8,9	11,15	19,25	6,10		
DG 201	4		5				13
NE 521		13		7		14	
AD 7226		3		5			18
LH0033	10						12
LH0132C	10						12
MC 1495	7						

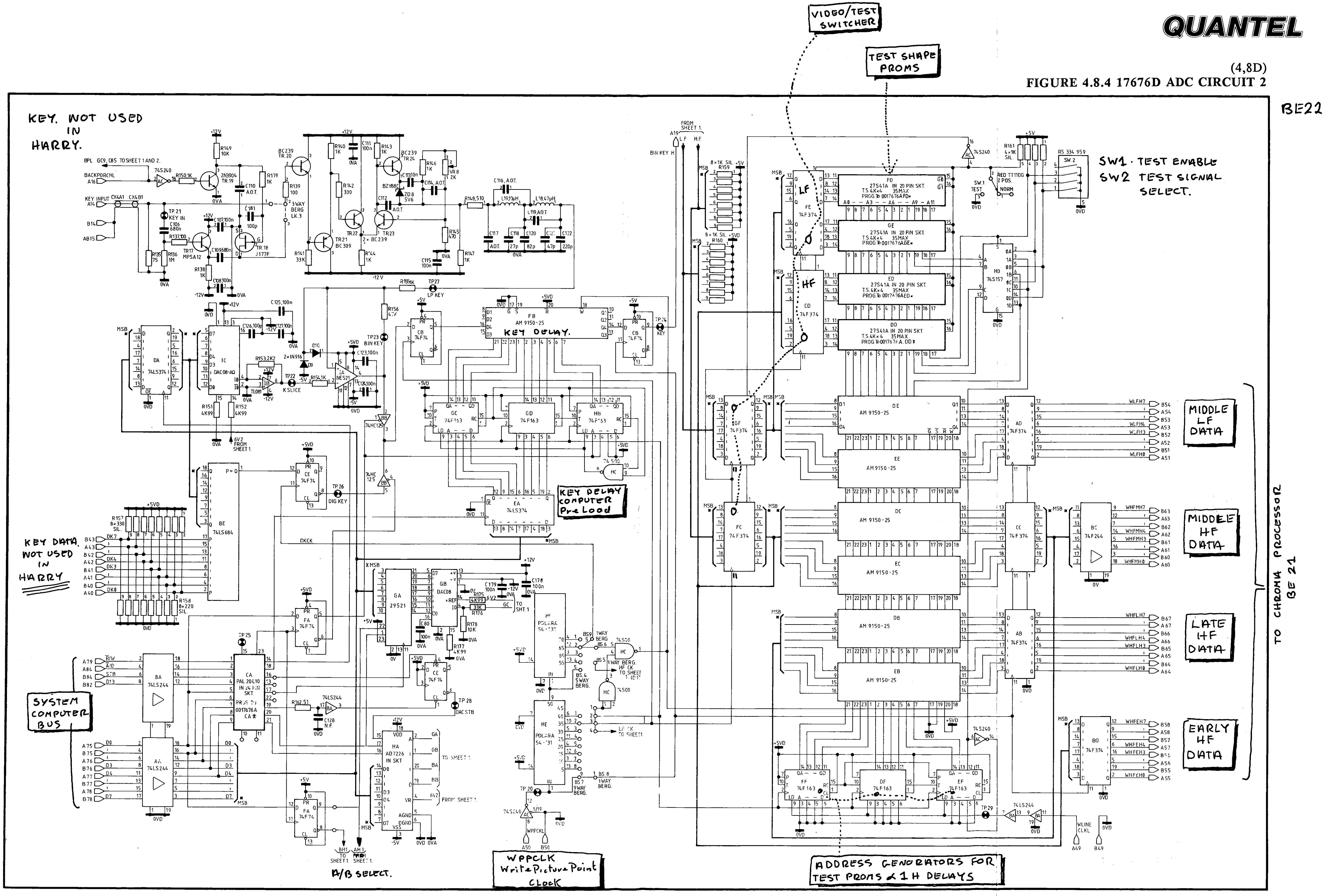
TYPE	-12V	0V	+5V	+12V
CA 3080	4			7
LM 348	11			4
HA 5033	5			1
14 PIN DIL		7	14	
16 PIN DIL		8	16	
20 PIN DIL		10	20	
24 PIN DIL		12	24	

TYPE	-12V	+12V
TL084 B	11	4
TL084 A	11	4

IC. POWER CONNECTIONS.

(4,8D)

FIGURE 4.8.4 17676D ADC CIRCUIT 2



INPUT OUTPUT STORE CARD 17710B

4:9:1 Function

The I/O Store is a video Frame store which is used to store and display the system's video output and menu display. The Store consists of two cards; one for luminance data and the other for U/V data.

Video data selected by the Input Switch card is stored in the I/O Store, controlled by the I/O Store Control card, and provides a full Frame of Luminance and U/V data for the Output Proc and RGB Output Proc cards.

4:9:2 Circuit Description

(a) DATA PATH

Luminance data from the Input Switch card is buffered by AL and clocked through the input registers (BL and BK for store stripe 0) and into the RAMs CC, CD, CE, CF, CG, CH, CI and CJ (for stripe 0). The data is then written into the location, addressed by the I/O Store Control card.

Data Read from the RAMs CC, CD, CE, CF, CG, CH, CI and CJ (for stripe 0) is clocked through the output registers BB and BA (for stripe 0) and enabled onto the inputs of the registers AB and AA. The output data is then clocked through and passed to the Output Proc and RGB Output Proc cards.

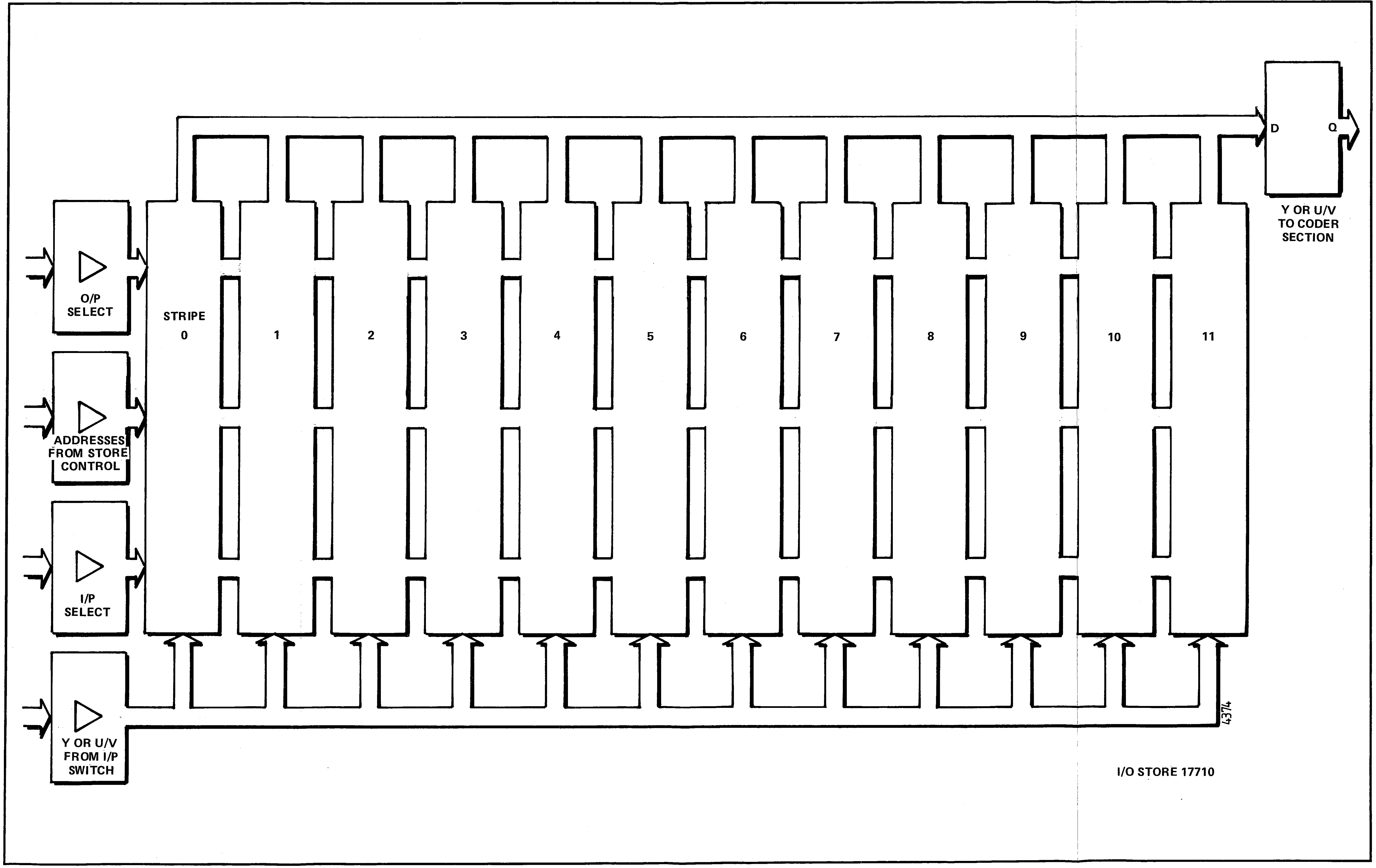
(b) STORE ADDRESSING

Input enable signals from the I/O Store Control card are buffered by AI and AJ, and clocked through the registers BI and BJ. These signals are passed to the Input registers on each store stripe to control when data is written into the RAMs.

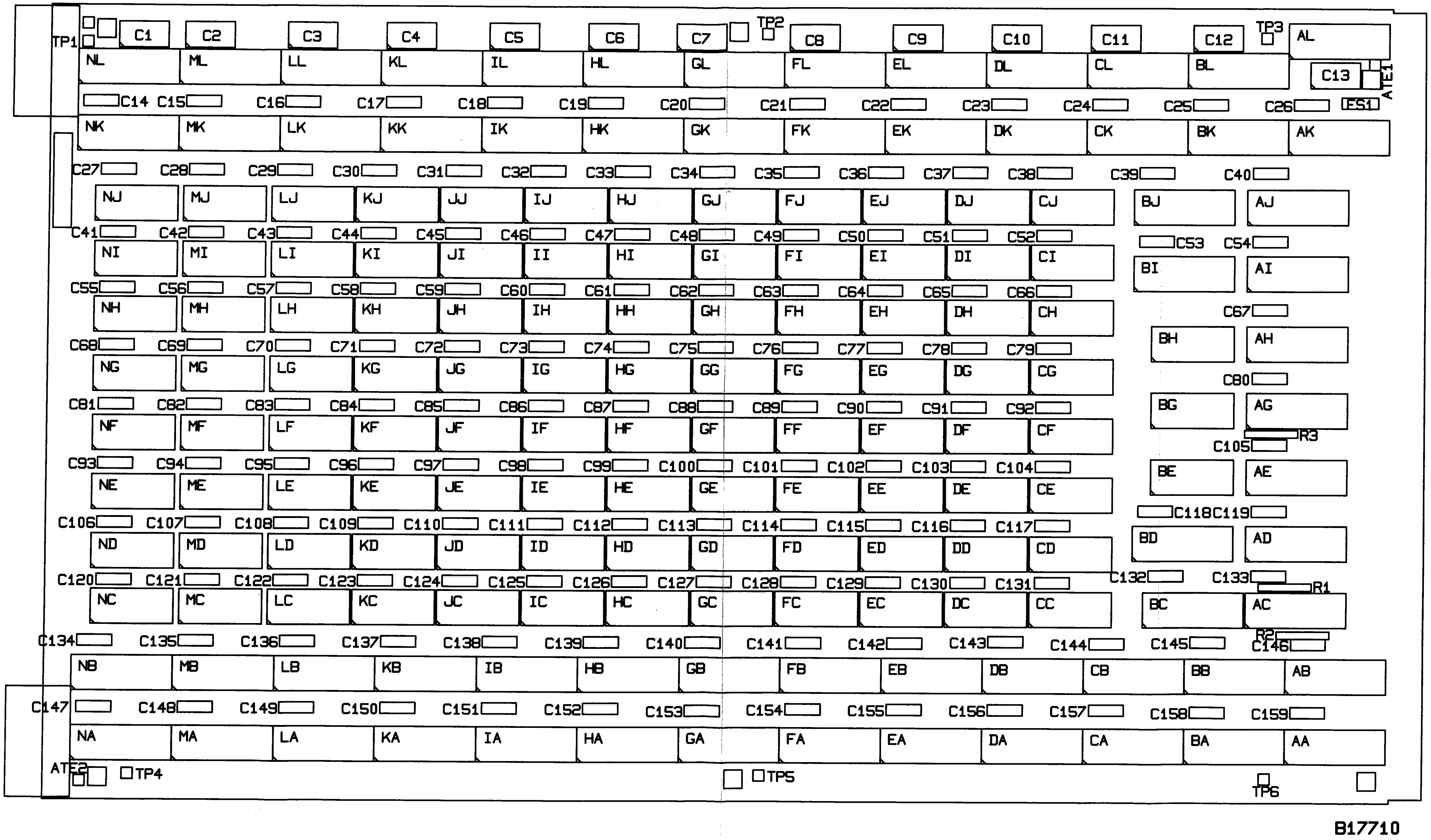
Output enable signals from the I/O Store Control card are buffered by AC and AD, and clocked through the registers BC and BD. These signals are passed to the Output registers on each store stripe to control when data is enabled onto the inputs of the registers AB and AA.

The store addresses from the I/O Store Control card are buffered by AE, AG and AH, and passed to the address inputs of all the RAMs.

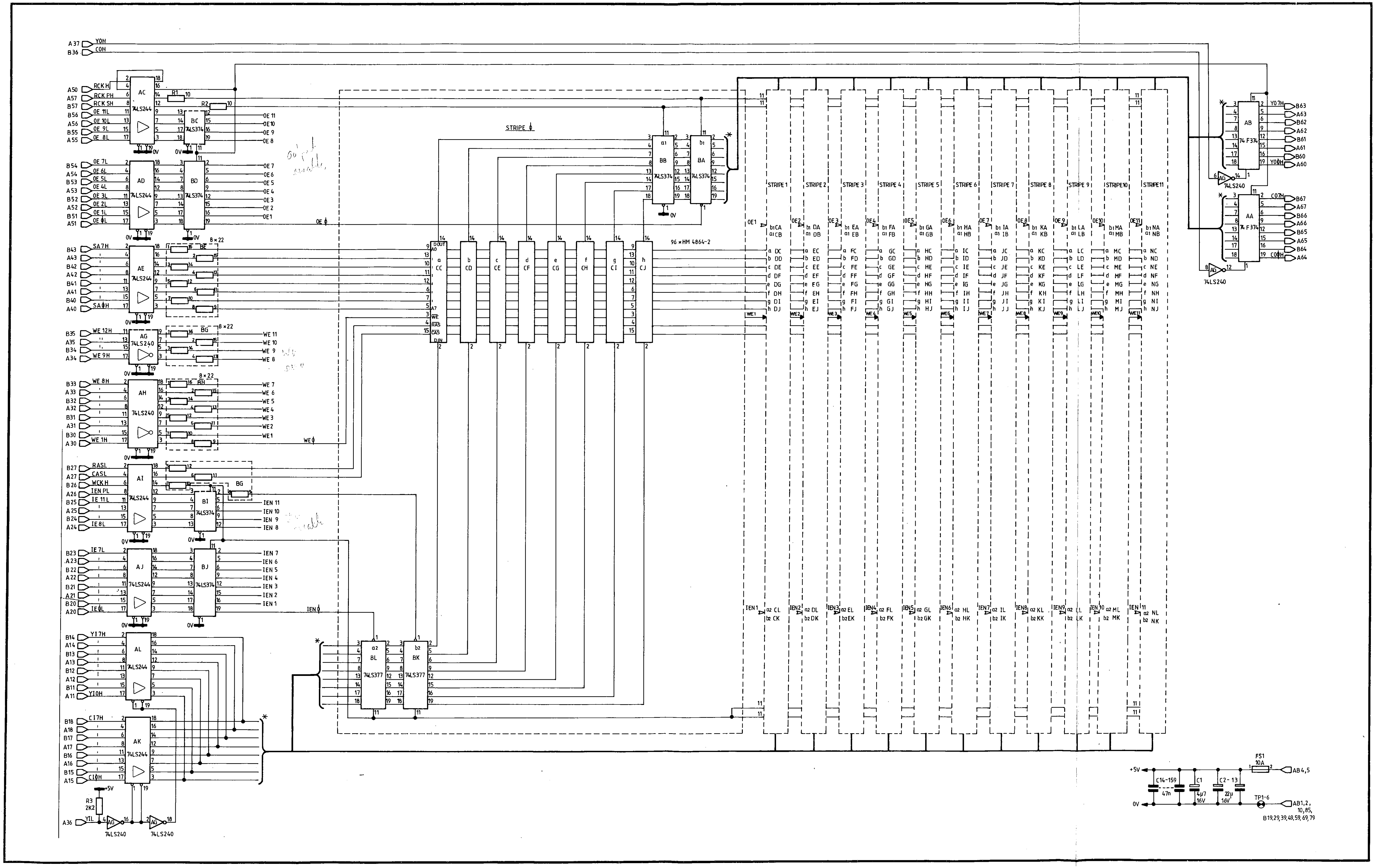
(4,9B)
FIGURE 4.9.1 17710B I/O STORE BLOCK



(4,9B)
FIGURE 4.9.2 17710B I/O STORE LAYOUT


TP1 C1 C2 C3 C4 C5 C6 C7 TP2 C8 C9 C10 C11 C12 TP3 AL
NL ML LL KL IL HL GL FL EL DL CL BL C13 ATE1
C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 FS1
NK MK LK KK IK HK GK FK EK DK CK BK AK
C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40
NJ MJ LJ KJ JJ IJ HJ GJ FJ EJ DJ CJ BJ AJ
C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54
NI MI LI KI JI II HI GI FI EI DI CI BI AI
C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67
NH MH LH KH JH IH HH GH FH EH DH CH BH AH
C68 C69 C70 C71 C72 C73 C74 C75 C76 C77 C78 C79 C80
NG MG LG KG JG IG HG GG FG EG DG CG BG AG
C81 C82 C83 C84 C85 C86 C87 C88 C89 C90 C91 C92 R3 C105
NF MF LF KF JF IF HF GF FF EF DF CF
C93 C94 C95 C96 C97 C98 C99 C100 C101 C102 C103 C104
NE ME LE KE JE IE HE GE FE EE DE CE BE AE
C118 C119
C106 C107 C108 C109 C110 C111 C112 C113 C114 C115 C116 C117
ND MD LD KD JD ID HD GD FD ED DD CD BD AD
C132 C133 R1
C120 C121 C122 C123 C124 C125 C126 C127 C128 C129 C130 C131
NC MC LC KC JC IC HC GC FC EC DC CC BC AC
R2
C134 C135 C136 C137 C138 C139 C140 C141 C142 C143 C144 C145 C146
NB MB LB KB IB HB GB FB EB DB CB BB AB
C147 C148 C149 C150 C151 C152 C153 C154 C155 C156 C157 C158 C159
NA MA LA KA IA HA GA FA EA DA CA BA AA
ATE2 TP4 TP5 TP6
B17710

(4,9B)
FIGURE 4.9.3 17710B I/O STORE CIRCUIT



DISK CONTROLLER CARD 17711D

4:10:1 Function

The function of this card is to convert instructions from the system computer into Disk control information. This card uses a bit slice sequencing element to provide the addresses for a 64-bit wide micro code word held in RAM on the card. This micro code word controls the operation of the Disk Drive; setting up the Disk when data transfer between the Disk and the system is required.

4:10:2 Circuit Description

(a) SYSTEM BUS DECODING

The system computer bus is buffered by BA, AA and AB, and decoded by the Prom CA and the PAL BB to provide the clocks and enables for the computer controlled circuitry on this card. The data from the bus is passed to computer loaded registers and FIFOs which control the operation of the card. Data is loaded in these registers and FIFOs when enabled by the PAL BB and associated decoding circuitry.

The FIFO Circuit JE, DA, FA and GE is loaded by the system computer with the instructions to be carried out by the Disk Controller at the next Disk access. These instructions determine the type of Disk access and the location on the Disk that is to be accessed.

(b) LOADING MICRO CODE PROGRAM

On system power up or reset, data is passed through the selected bi directional buffer NB, MB, LB, KB, JB, IB, HB or GB enabled by IA. Each buffer is enabled in turn, so that data from the system bus is passed to the inputs of the appropriate RAM. Each 8-bit word from the system bus is then written into the addressed location of RAM with Write Enables from JA.

During the loading process the RAMs are addressed by the counter circuit DE, DC, DB and FF, which is loaded prior to data transfer with the address start value from the system computer bus.

The 64-bit wide micro code loaded into the RAM is checked by the system computer, which reads the data back via the bi directional buffers NB to GB.

(c) MICRO CODE OPERATION

During normal system operation the bit slice sequencing element NE provides the addresses for the micro code RAMs. Each word of the micro code is registered before being used to control the card.

The words from the registers ND and MD are passed to the Bit slice element NE to provide any jump addresses required by the sequencer. Four bits from MD are passed through ME, which allows the sequencer to be reset.

The word from the register LD controls the 32-bit Multiplexer circuit LE, KE, IF and JF, which provides 32 condition code inputs for NE. The registers LD and KD provide a 10-bit command word which is sent to the Disk (Bus) via the register EC and the TTL-ECL converters AC, BC and BF and to the Disk (Radial) via the register EF and the TTL-ECL converters AF.

The register JD provides various control signals which are passed to the Disk via the TTL-ECL converters AG (Radial). The register ID provides various control signals which control the system computer bus while the Disk Controller is operating.

The register HD controls the 3 counter circuits; NA, MA and OA, OF, OE and QE, and PE, PF and QF. These counters are loaded with the complementary values of "lines per sector" and "Pixels per line", from the computer loaded registers OB and PB (counter 1), OD and PC (counter 2) and PD and PA (counter 3). The carry outputs from these counter circuits are passed to the selector JF in the multiplexer circuit.

The word from the register FB is buffered by CB and passed to the Disk Interface card to control the Disk data transfer.

(d) DISK STATUS

The status signals from the Disk (Bus) are buffered by the TTL-ECL converters and then passed to selectors LE and KE of the Multiplexer circuit.

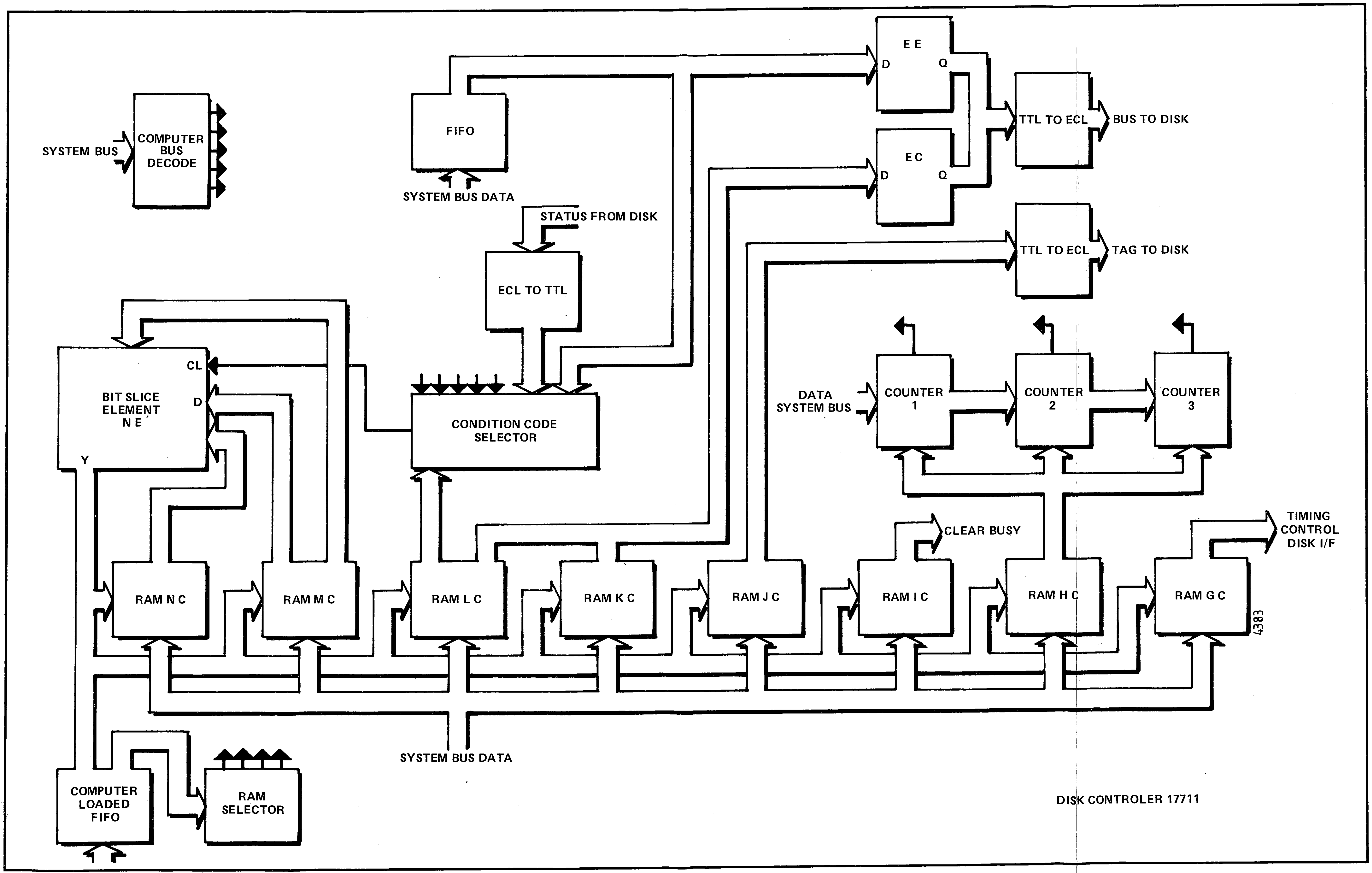
The Disk status signals are also read by the system computer bus via the buffer CF, should a fault condition occur.

(e) DISPLAYS

The LED displays on this card display the RAM address of the selected word of micro code. The Green LED on the Front of the card indicates (when on) that the Disk Controller is operating.

(4,10D)

FIGURE 4.10.1 17711D DISK CONTROLLER BLOCK



(4,10D)

FIGURE 4.10.2 17711D DISK CONTROLLER LAYOUT

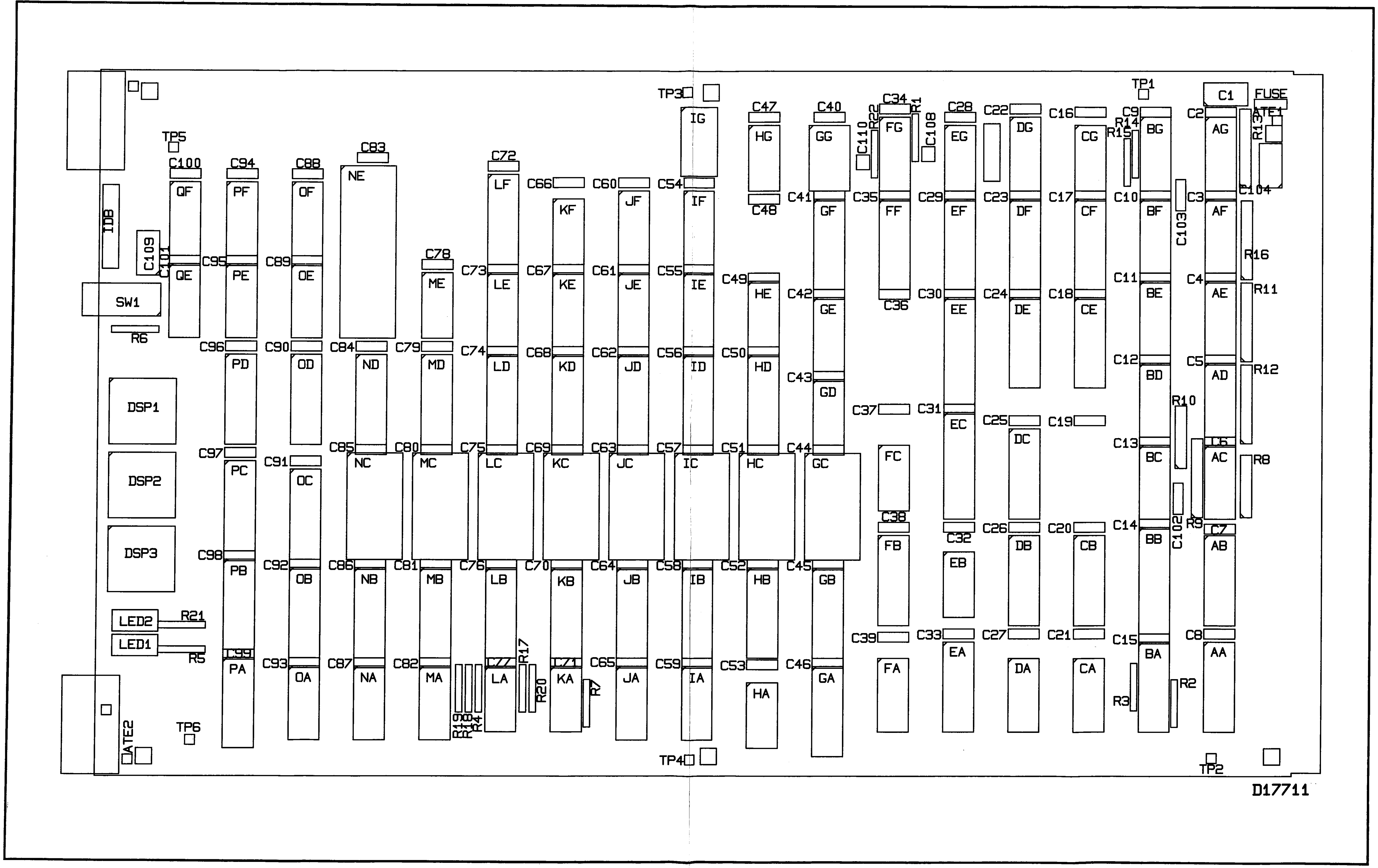
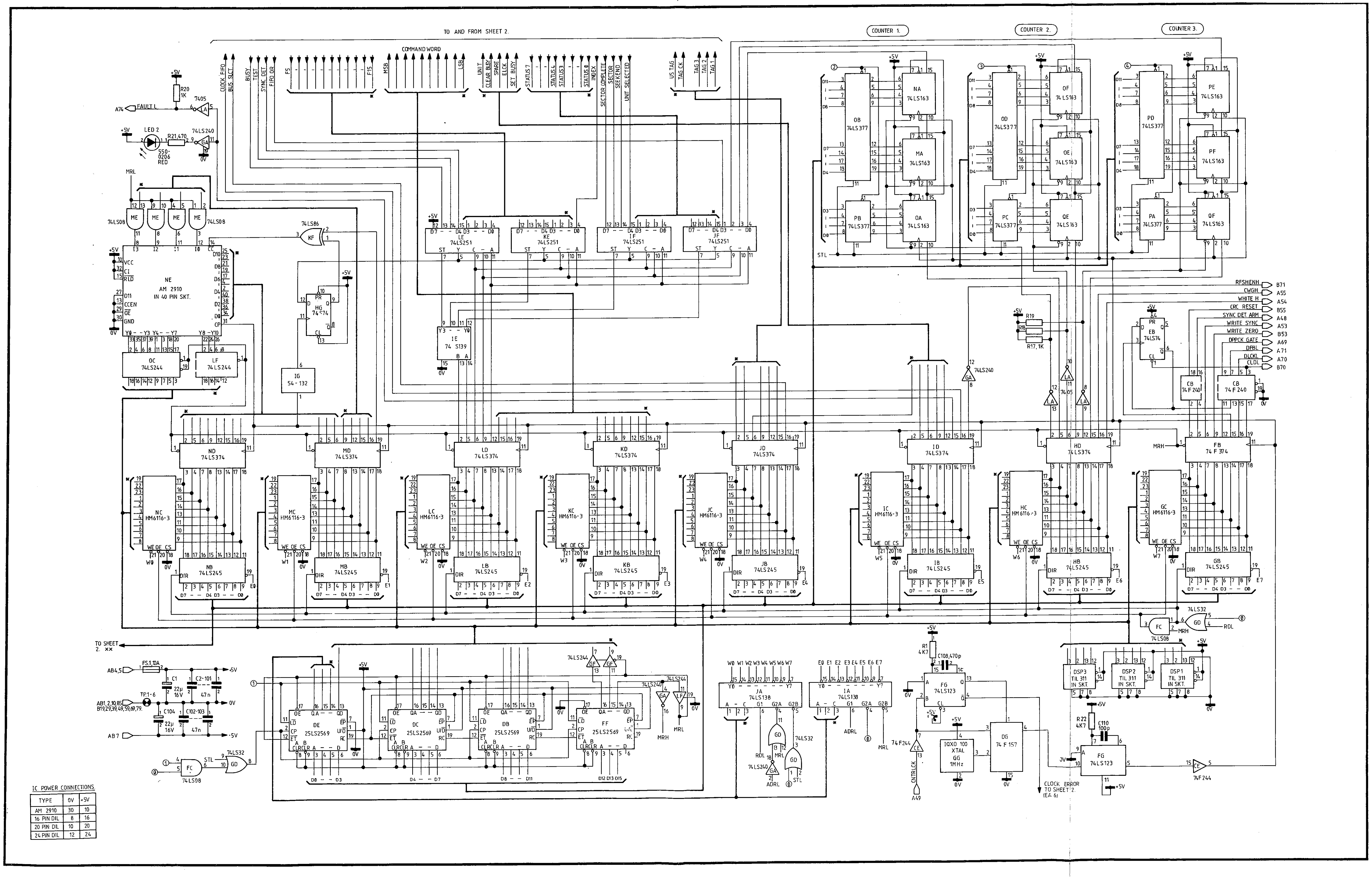


FIGURE 4.10.3 17711D DISK CONTROLLER CIRCUIT 1

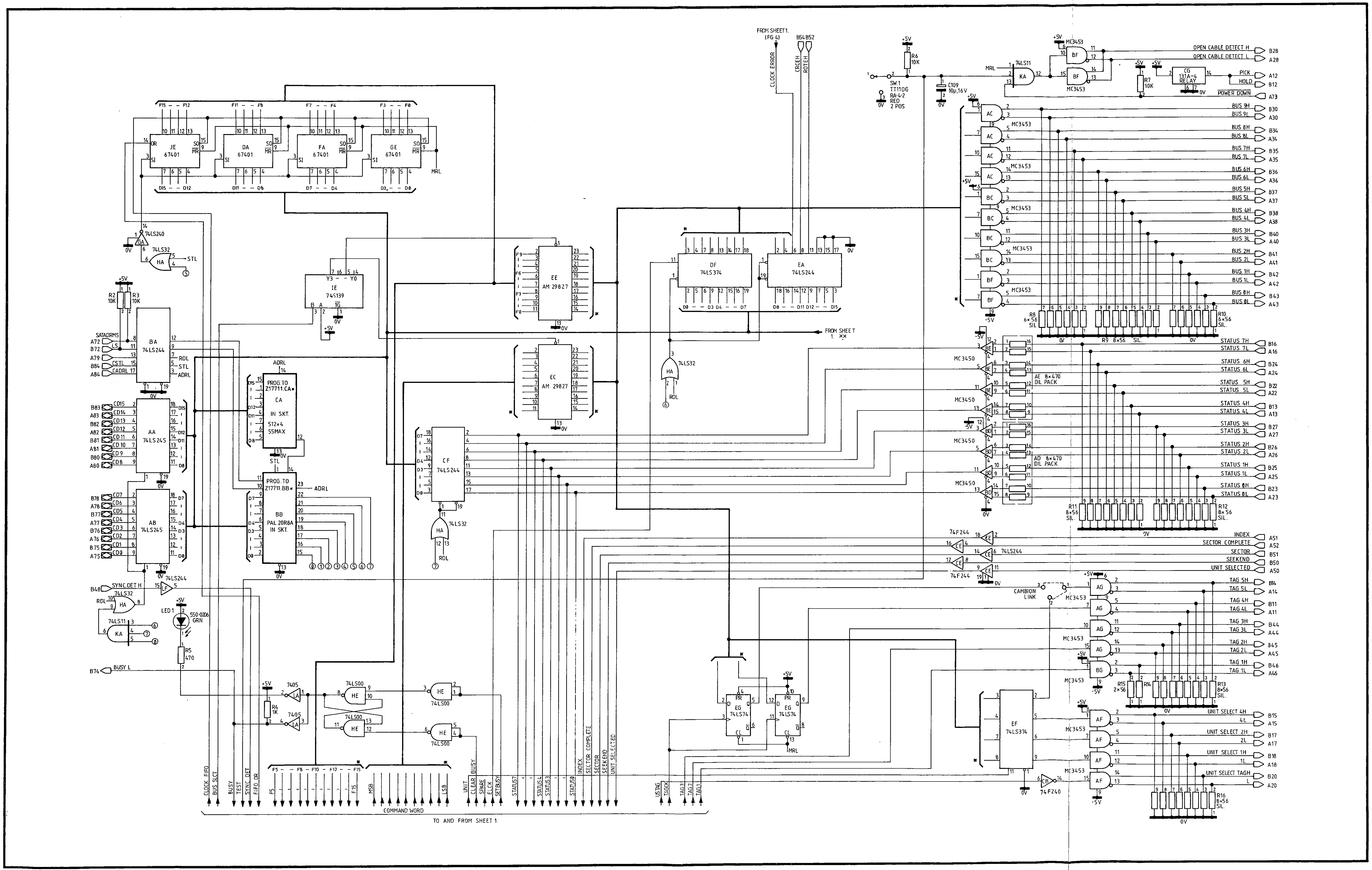


IC POWER CONNECTIONS.

TYPE	0V	+5V
AM 2910	30	10
16 PIN DIL	8	16
20 PIN DIL	10	20
24 PIN DIL	12	24

(4,10D)

FIGURE 4.10.4 17711D DISK CONTROLLER CIRCUIT 2



DISK INTERFACE CARD 17713C

4:11:1 Function

There are four Disk Interface cards in the system; one for each Disk Drive. Each Disk Interface card interfaces the parallel data format used in its satellite with the 5 serial data paths provided by the Disk Drive.

The function of this card is to interface the Disk drive data path with the system. The system provides data in 8-bit word format which has to be converted into 5 serial data streams which correspond directly with the 5 parallel Heads on the the PTD Disk Drive.

4:11:2 Circuit Description

(a) DATA PATH TO DISK

Data from the satellite Buffer Store is passed via the Data Select card to the Disk Interface card. This data is clocked through the register AA into one of the five registers GA, FA, EA, DA or CA in the de-multiplexer circuit.

The selected data from these registers is clocked into the parallel inputs of the shift registers GB, FB, EB, DB and CB. The serial data produced by these shift registers is buffered by BB and passed through CF, DF, EF, GF and FF to the TTL-ECL converters BJ and AJ. The complimentary ECL data produced is then passed to the Disk Drive via the Radial cable.

The buffer BA is enabled onto the inputs of AA so that sector sync words can be written onto the Disk.

(b) DATA PATH FROM DISK

Serial ECL data from the Disk Drive is buffered by the ECL-TTL converters BH and BI, and the serial data is clocked into the shift registers CD, DD, ED, FD and GD. The five 8-bit words produced are clocked into the registers CC, DC, EC, FC and GC in the multiplexer circuit. Then enabled in turn to produce continuous parallel data. This data is clocked through the register BC, buffered by AC and then passed to the Data select card.

The 8-bit word produced by the shift register CD is decoded by CG and CE to provide Disk sync word detection. When a sync word is detected CI passes the Sync detect flag to the Disk.

(c) MULTIPLEXER CONTROL CIRCUITRY

The Disk bit rate clocks are buffered by BF and passed through the delay line EI. The delayed outputs of EI are tapped to produce 2 pulses each bit clock on the output of EH. These pulses clock the shift registers DG and EG, and the counters DE, EE, FE and GE to produce control signals for the Multiplexer and De-multiplexer circuits. The counter circuit enables the outputs of the registers GA to CA (for Disk Writes) or CC to GC (for Disk Reads).

(d) CONTROL SIGNAL PATHS

Various Disk control signals from the Radial cable are buffered by the ECL-TTL converters BF and BG, and are then passed to the Disk Controller card via the buffer AE.

(4,11C)
FIGURE 4.11.1 17713C DISK INTERFACE BLOCK

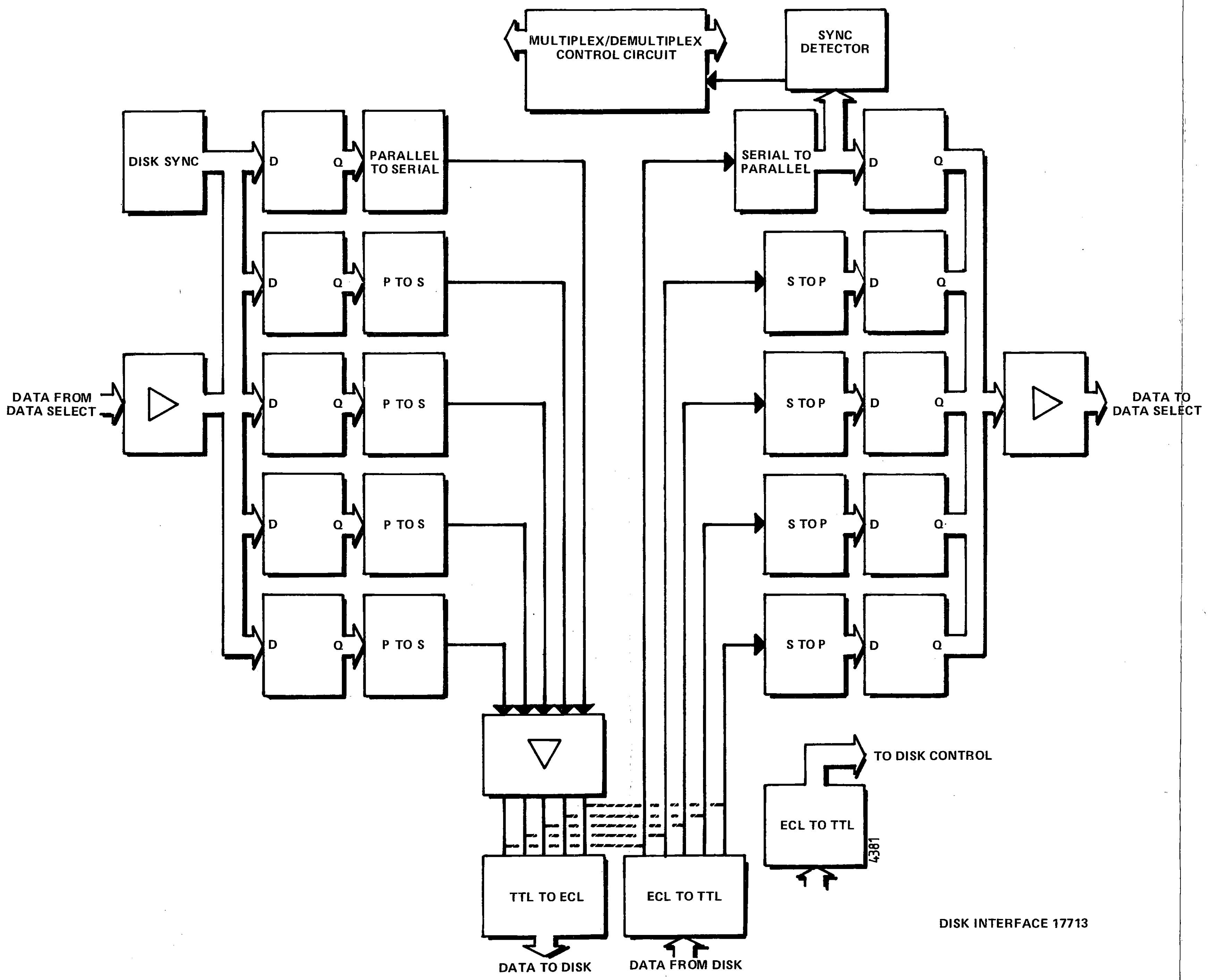


FIGURE 4.11.2 17713C DISK INTERFACE LAYOUT

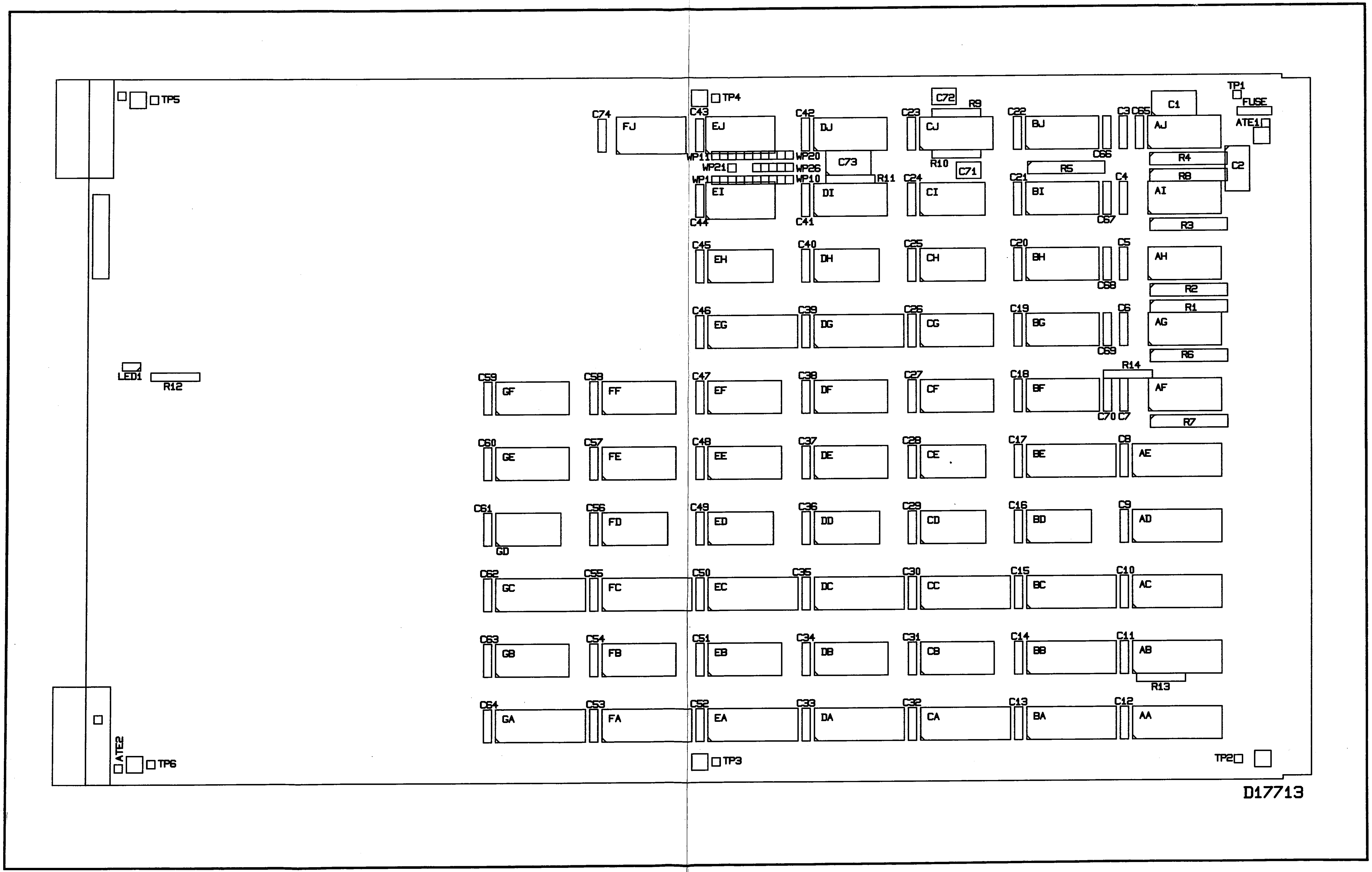
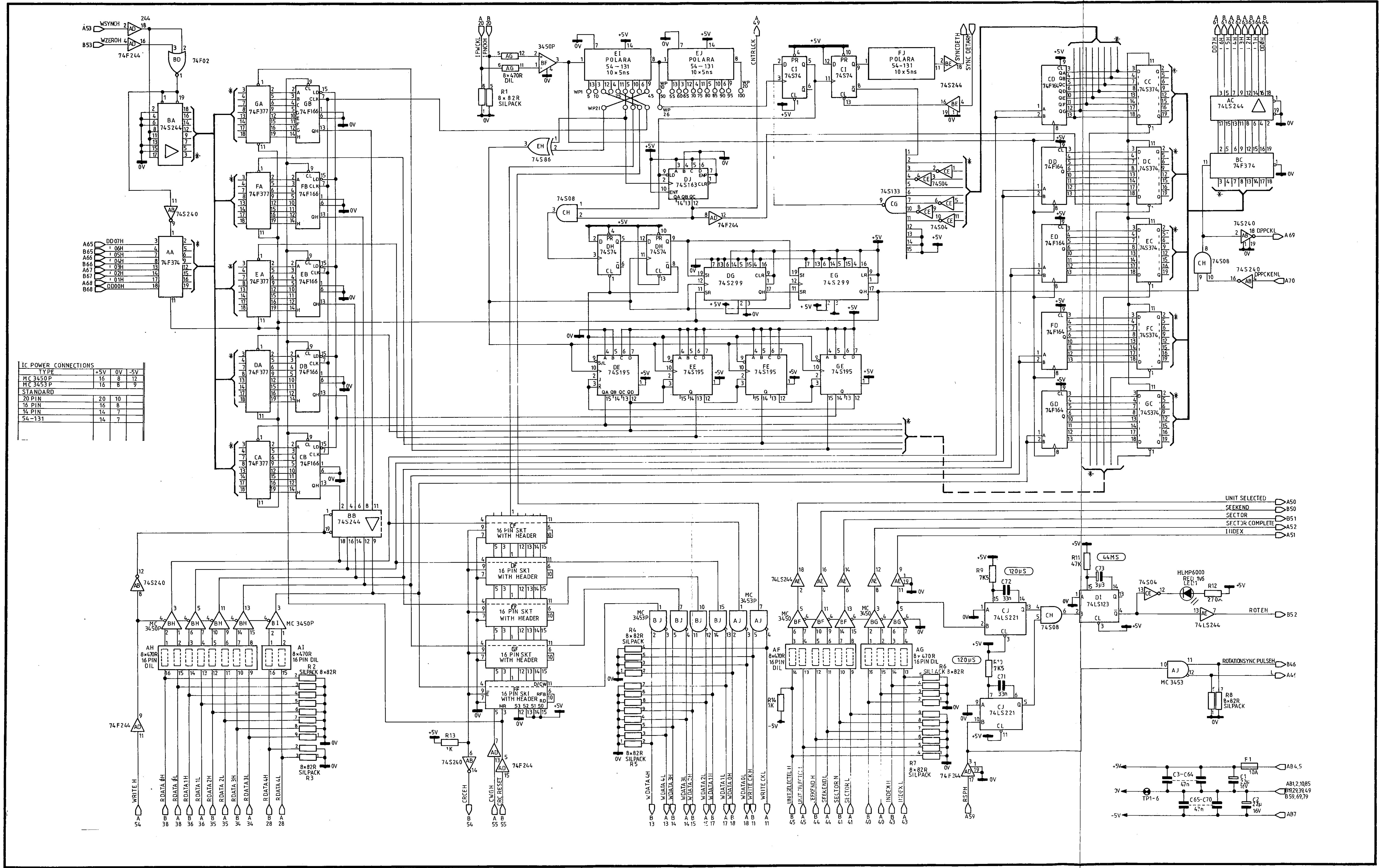


FIGURE 4.11.3 17713C DISK INTERFACE CIRCUIT



IC POWER CONNECTIONS

TYPE	+5V	0V	-5V
MC 3450 P	16	8	12
MC 3453 P	16	8	9
STANDARD			
20 PIN	20	10	
16 PIN	16	8	
14 PIN	14	7	
54-131	14	7	

BUFFER STORE CARD 17715B

4:12:1 Function

The function of the Buffer Store is to hold satellite data while it is being written into or read from the satellite Disc Drive. The store consists of two Buffer Store cards each holding 3 BUFFERS A, B and C which have 4 store stripes.

Data is written to a buffer on one video field then read out on the next video field.

4:12:2 Circuit Description

(a) WRITE DATA PATH; Buffers A [B] {C}

Data from the output of the Combiner card or from the Data select card is buffered by I3B or I2A onto the inputs of the buffers I8I and I5I [I8E and I5E] {I8A and I5A}.

The data is selected for one of the BUFFERS A, B or C and enabled onto the inputs of the selected store stripe input registers I8J, I14J, I20J and I26J [I8F, I14F, I20F and I26F] {I8B, I14B, I20B and I26B}.

The data from the input registers is clocked through the registers I8K, I14K, I20K or I26K [I8G, I14G, I20G or I26G] {I8C, I14C, I20C or I26C} when enabled. The data from the these registers is then written sequentially into each stripe of RAM.

(b) READ DATA PATH; Buffers A [B] {C}

Data read from the selected BUFFER A, B or C is clocked into the stripe output registers I11K, I17K, I23K and I26I [I11G, I17G, I23G and I26E] {I11C, I17C, I23C and I26A}. Then the data from these registers, on the selected BUFFER A, B or C, is clocked onto the output bus through the registers I11J, I17J, I23J or I23I [I11F, I17F, I23F or I23E] {I11B, I17B, I23B or I23A}.

Data from the enabled register on the selected BUFFER A, B or C is clocked through the register I11I for BUFFER A, I11E for BUFFER B and I11A for BUFFER C, and then passed to the Combiner card. Data from each BUFFER is also selected onto a common output bus via the registers I14I, I14E and I14A and passed to the Data Select card.

(c) STORE ADDRESSING (Address 2 / Address 1)

Addresses from the Store Address card are buffered by I1E/I1B, and passed to the selected BUFFER A, B or C via the buffers I4G/I3G, I4E/I3E, and I4C/I3C. The addresses from these buffers are then passed to the address inputs of each RAM stripe in the appropriate BUFFER A, B and C.

Input Enables and clocks from the Store Address card are buffered by I1C/I1F and then passed to the buffers I2F/I2G, I2D/I2E and I2B/I2C for BUFFERS A, B and C. The outputs from the buffers I2F/I2G, I2D/I2E and I2B/I2C are then passed to the stripe input and output registers to control which stripe is written into.

Write Enables and RAS/CAS from the Store Address card are buffered by I3D/I1D and then passed to the buffers I5J/I5K, I5F/I5G and I5B/I5C for BUFFERS A, B and C. The outputs from the these buffers are passed to RAS and CAS inputs of each RAM in the appropriate BUFFER.

FIGURE 4.12.1 17715B BUFFER STORE BLOCK

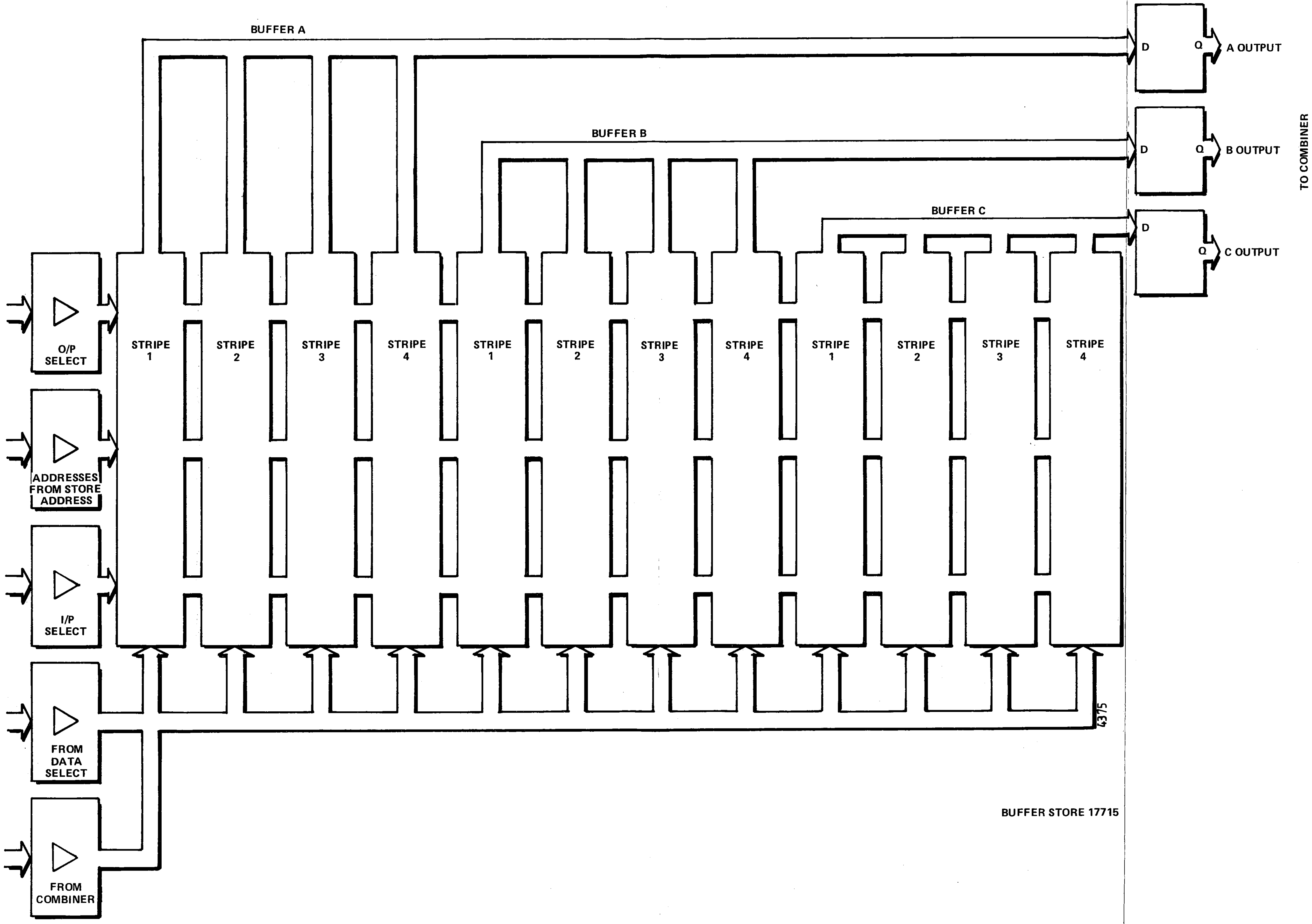
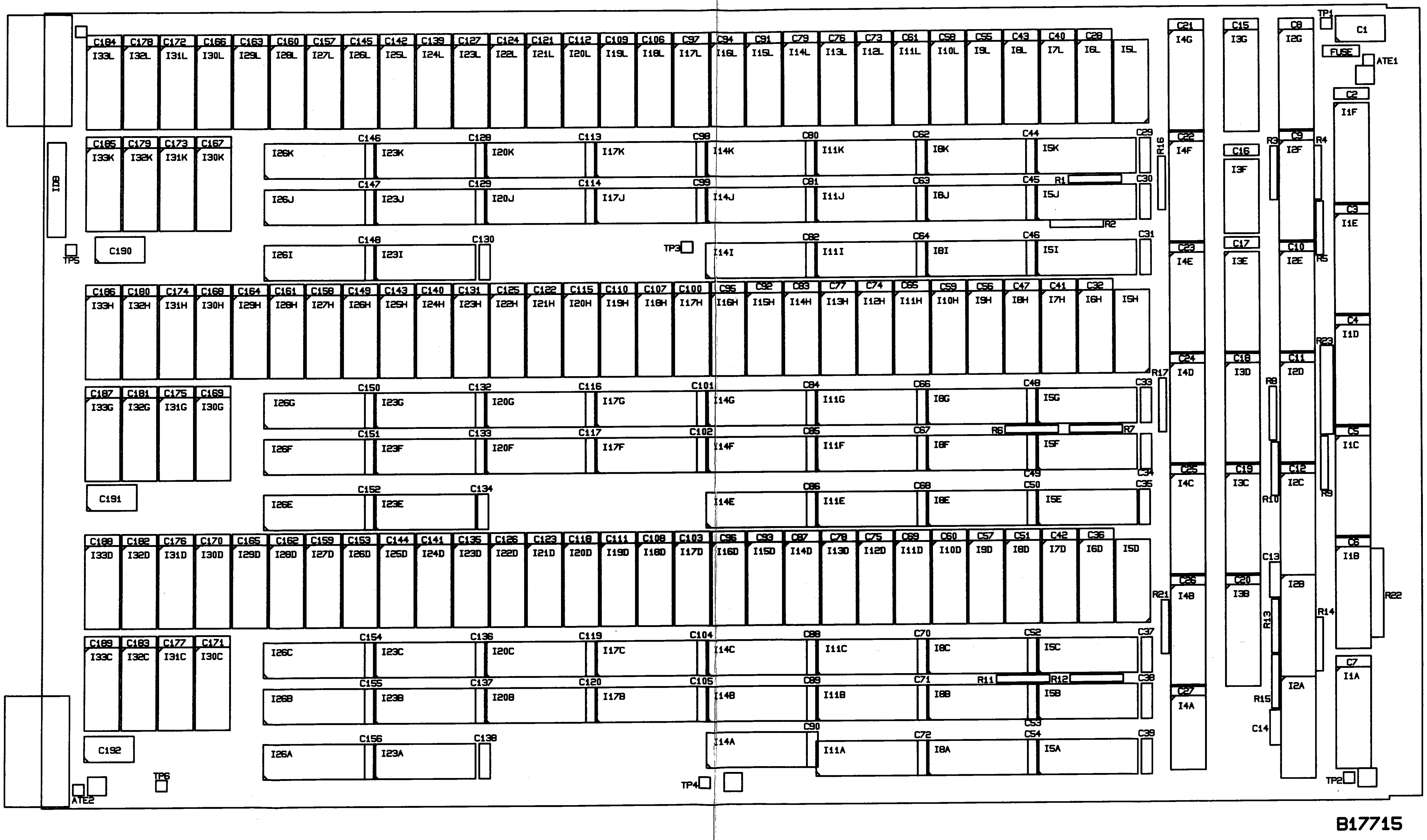
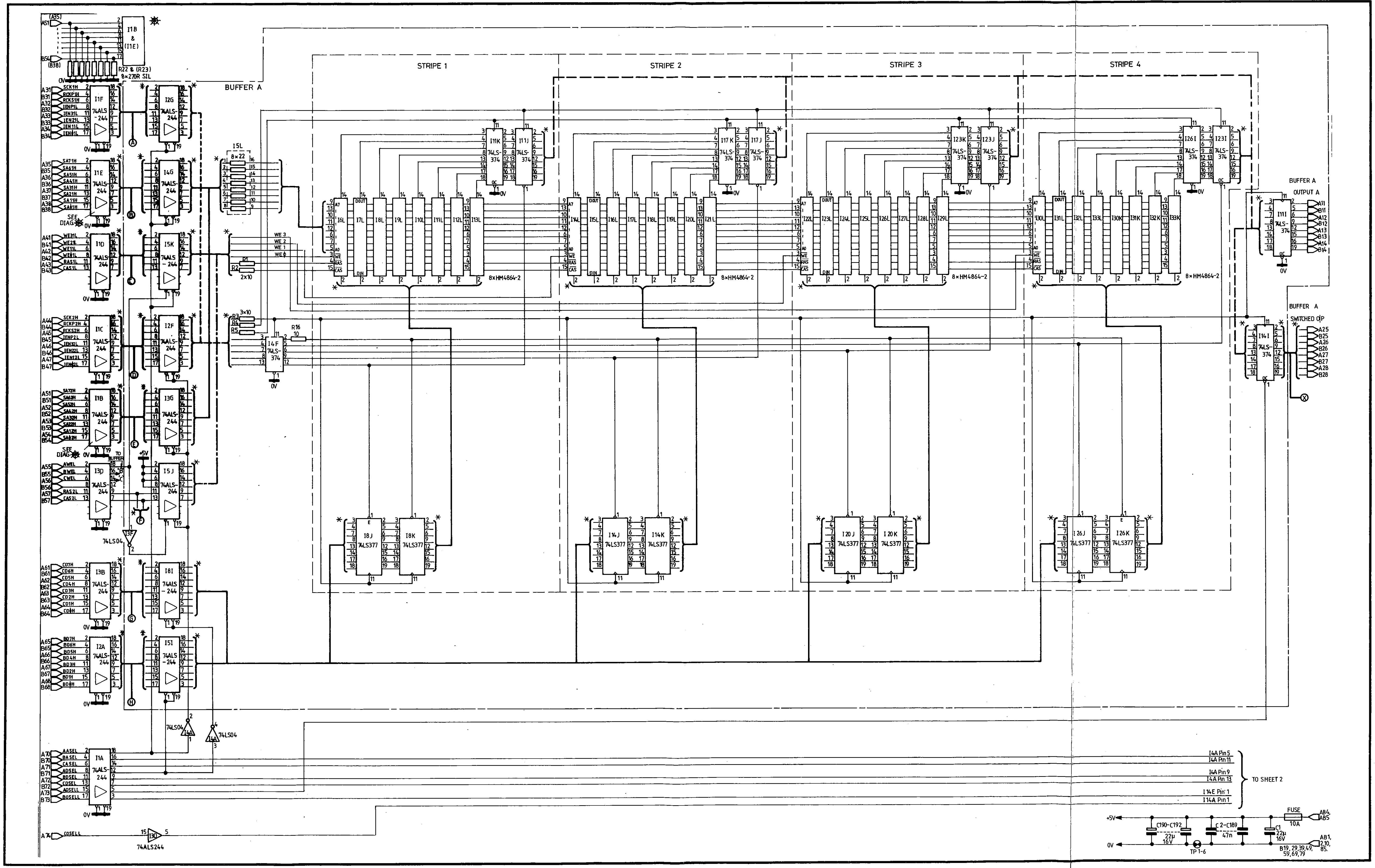


FIGURE 4.12.2 17715B BUFFER STORE LAYOUT



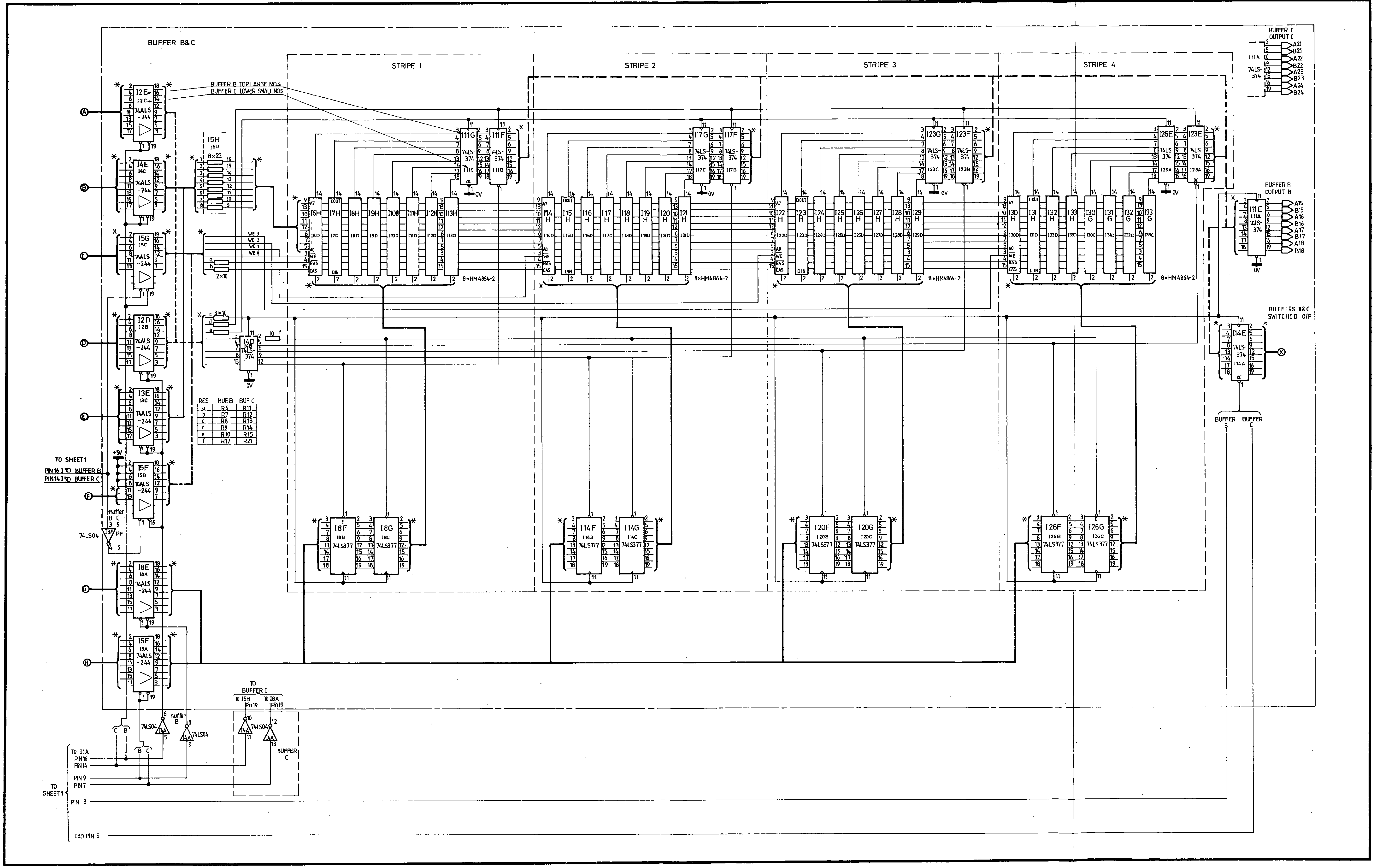
(4,12B)

FIGURE 4.12.3 17715B BUFFER STORE CIRCUIT 1



(4,12B)

FIGURE 4.12.4 17715B BUFFER STORE CIRCUIT 2



STORE ADDRESS CARD 17716F

4:13:1 Function

The function of this card is to provide the read and write addresses for the satellite Buffer cards. The addresses control the writing and reading of data to and from the Disk. The Store Address card consists of two similar address generator circuits which can be used for either read or write addressing. Although for nearly all operations the two circuits are dedicated to one function.

4:13:2 Circuit Description

(a) WRITE ADDRESS GENERATION

The counter circuit EK, FL and GL is clocked by picture point clocks (Disk or Video) and counts up from the loaded value held in the computer loaded FIFOs ED, FI and CC. The horizontal count produced by this circuit is passed to the store mapping circuit DJ, DL, BJ, CJ and DK.

The counter circuit FJ, GK and FK is clocked by line clocks (Disk or Video) and counts up from the loaded value held in the computer loaded FIFOs EF and GI. The vertical count produced by this circuit is passed to the store mapping circuit circuit DJ, DL, BJ, CJ and DK.

The mapped horizontal and vertical addresses from BJ, CJ and DK are passed to the Row and Column address registers BI and CI, which are enabled alternately onto an address bus. This bus is provided with refresh addresses from the register DI, buffered by AI and passed to the satellite Buffer Store cards.

(b) WRITE STORE CONTROL

The store cycle pulse from II is passed down the delay lines JL, JK and JJ to provide various delayed pulses. These pulses are combined by the logic IL, IK, IJ, JI and KF to produce the strobe and control signals for the address multiplexer circuit and for the Dynamic RAMs on the Buffer Store cards. The logic II, GJ and HJ controls the synchronizing of the store cycles with the Refresh circuit and with the system computer.

The decoder HK produces 4 input enable signals which control the input registers on the stripes of the Buffer Store cards. The logic EJ, EI, EH, AM and BF produces 4 write enable signal which control the writing of these stripes.

The FIFOs FD and DB are loaded by the system computer with the stripe select enables theses are buffered by AC and passed to the Buffer Store cards to control which stripes are to be enabled for writing.

(c) READ ADDRESS GENERATION

The counter circuit GF, GH and HF is clocked by picture point clocks (Disk or Video) and counts up from the loaded value held in the computer loaded FIFOs EE, FH and DA. The horizontal count produced by this circuit is passed to the store mapping circuit CF, DF, BH, CH and DH.

The counter circuit GD, GE and HD is clocked by line clocks (Disk or Video) and counts up from the loaded value held in the computer loaded FIFOs EC and FE. The vertical count produced by this circuit is passed to the store mapping circuit circuit CF, DF, BH, CH and DH.

The mapped horizontal and vertical addresses from BH, CH and DH are passed to the Row and Column registers BG and CG, which are enabled alternately onto an address bus. This bus is provided with refresh addresses from the register DG, buffered by AG and passed to the satellite Buffer Store cards. The Refresh addresses are produced by the counter circuit HH and HI, and passed to the inputs of the registers DI and DG.

(d) READ STORE CONTROL

The store cycle pulse from ID is passed down the delay lines IC, IB and IA to provide various delayed pulses. These pulses are combined by the logic HB, HA, JC, and JB to produce the strobe and control signals for the address multiplexer circuit and for the Dynamic RAMs on the Buffer Store cards. The logic ID, JD and IE controls the synchronizing of the store cycles with the Refresh circuit and with the system computer.

The decoder JF produces 4 input enable signals which control the input registers on the stripes of the Buffer Store cards.

(e) STORE REQUEST CIRCUITRY

The FIFOs DC, FF and BC, and EB, FG and BE in conjunction with the PALs CE and DE control which stripes on the Buffer Store cards are to be written on the next video field or Disk frame. The FIFOs are computer loaded with the enables for the next Buffer Store access and the PALs CE and DE ensure that the buffer selection occurs at the correct time.

(f) COMPUTER BUS DECODE

The system computer bus is buffered by BA, AA and AB, and decoded by the Prom BB and the PAL CB to provide the clocks and enables for the computer controlled circuitry on this card.

FIGURE 4.13.1 17716F STORE ADDRESS BLOCK

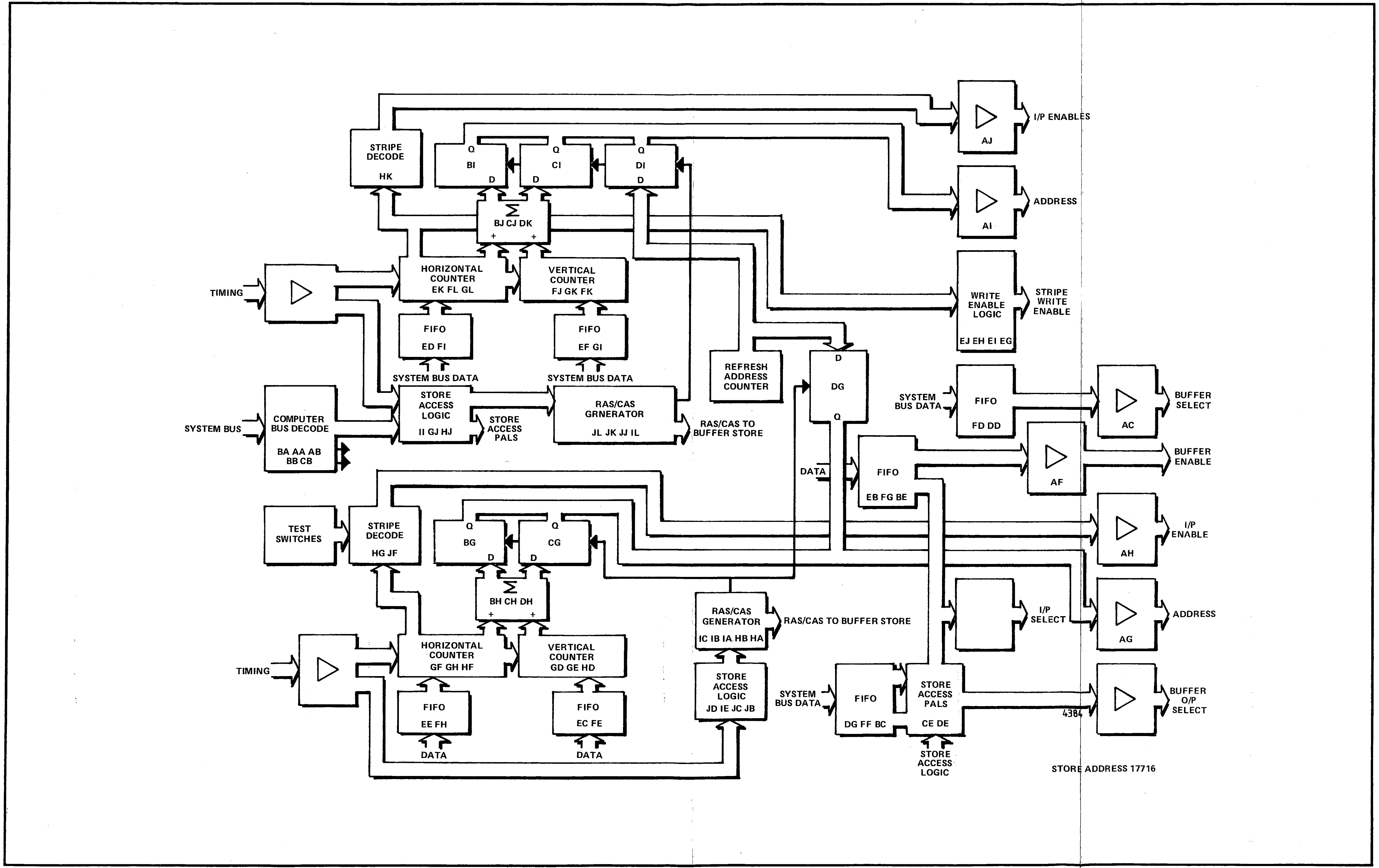
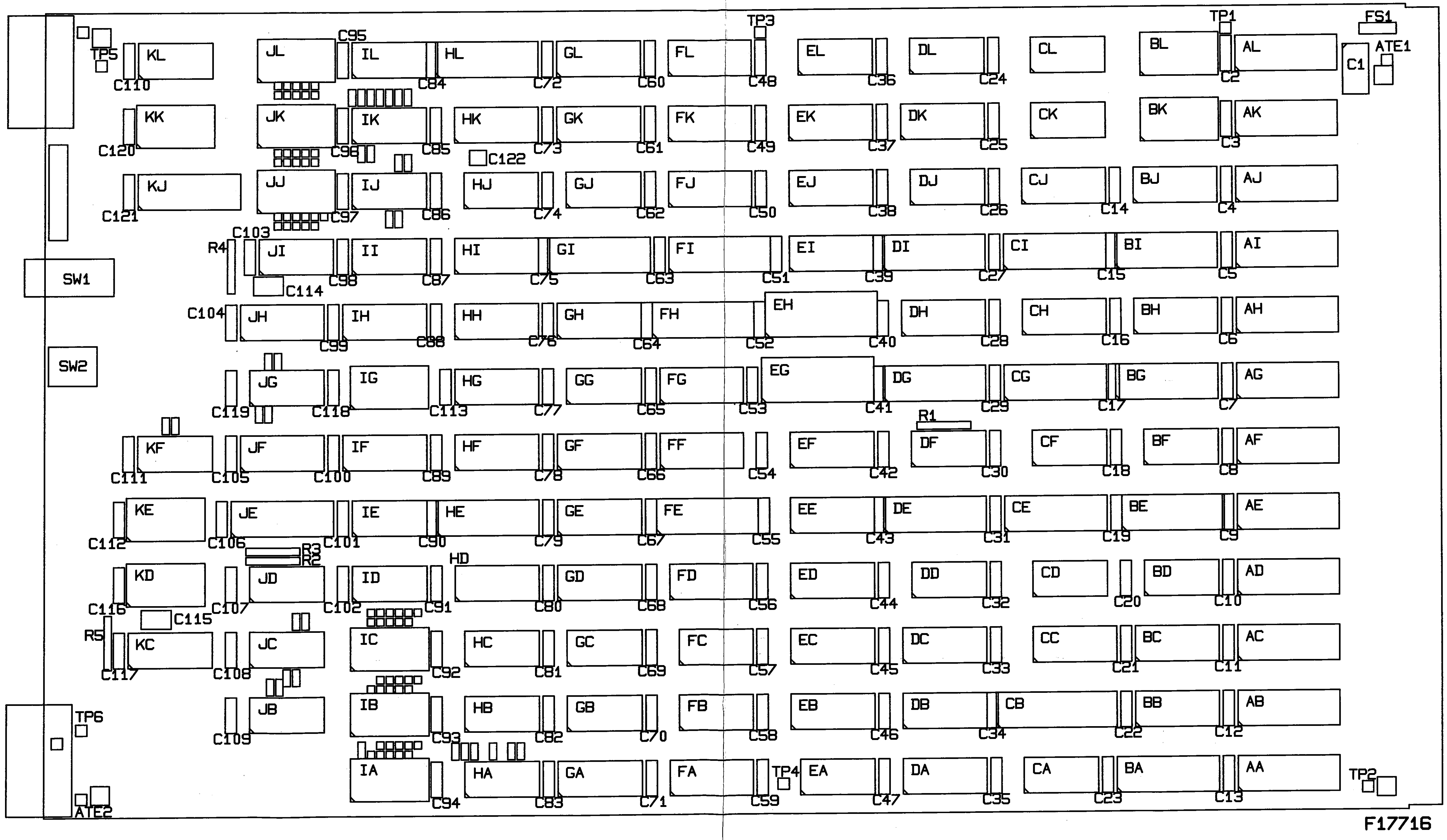
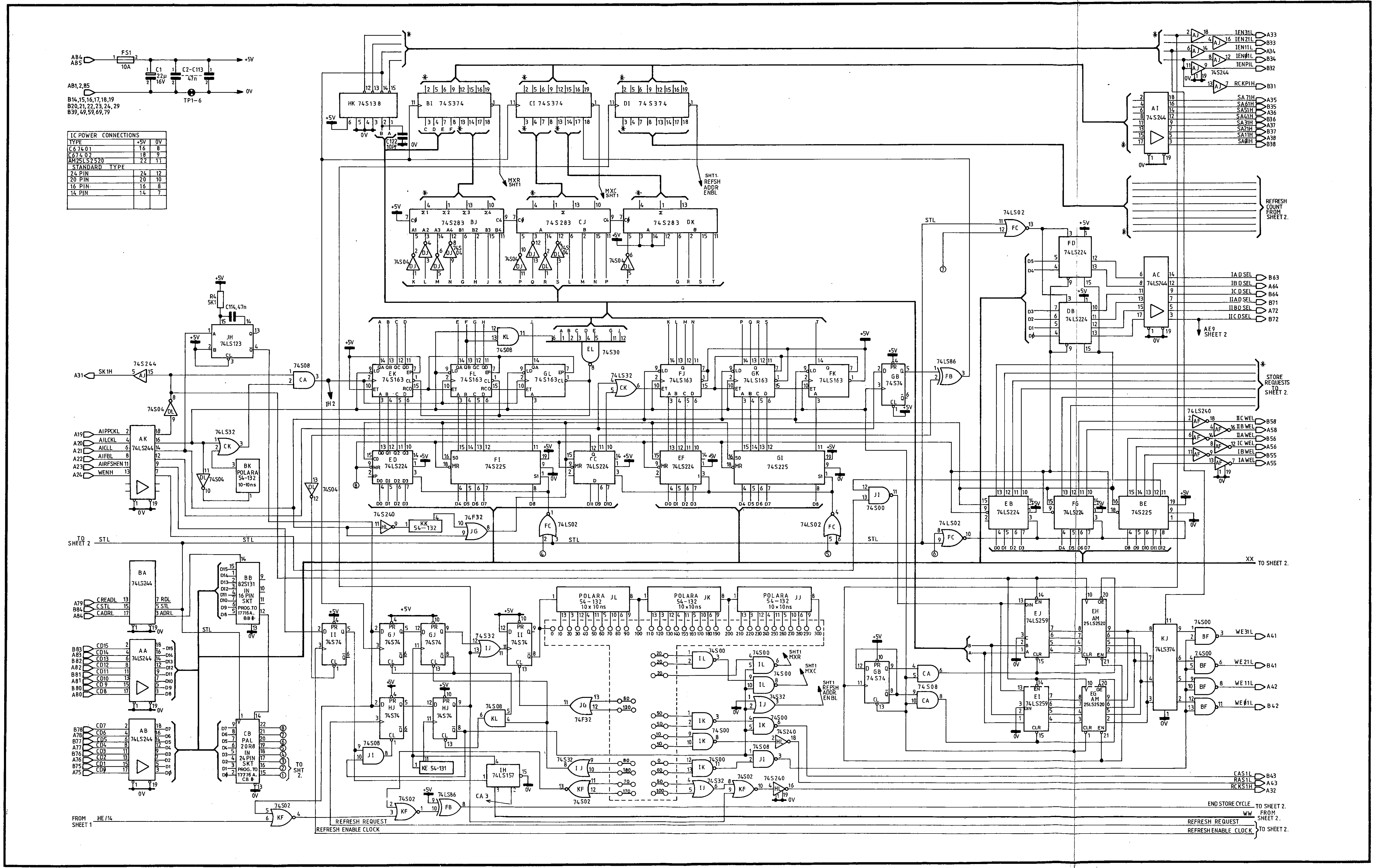


FIGURE 4.13.2 17716F STORE ADDRESS LAYOUT



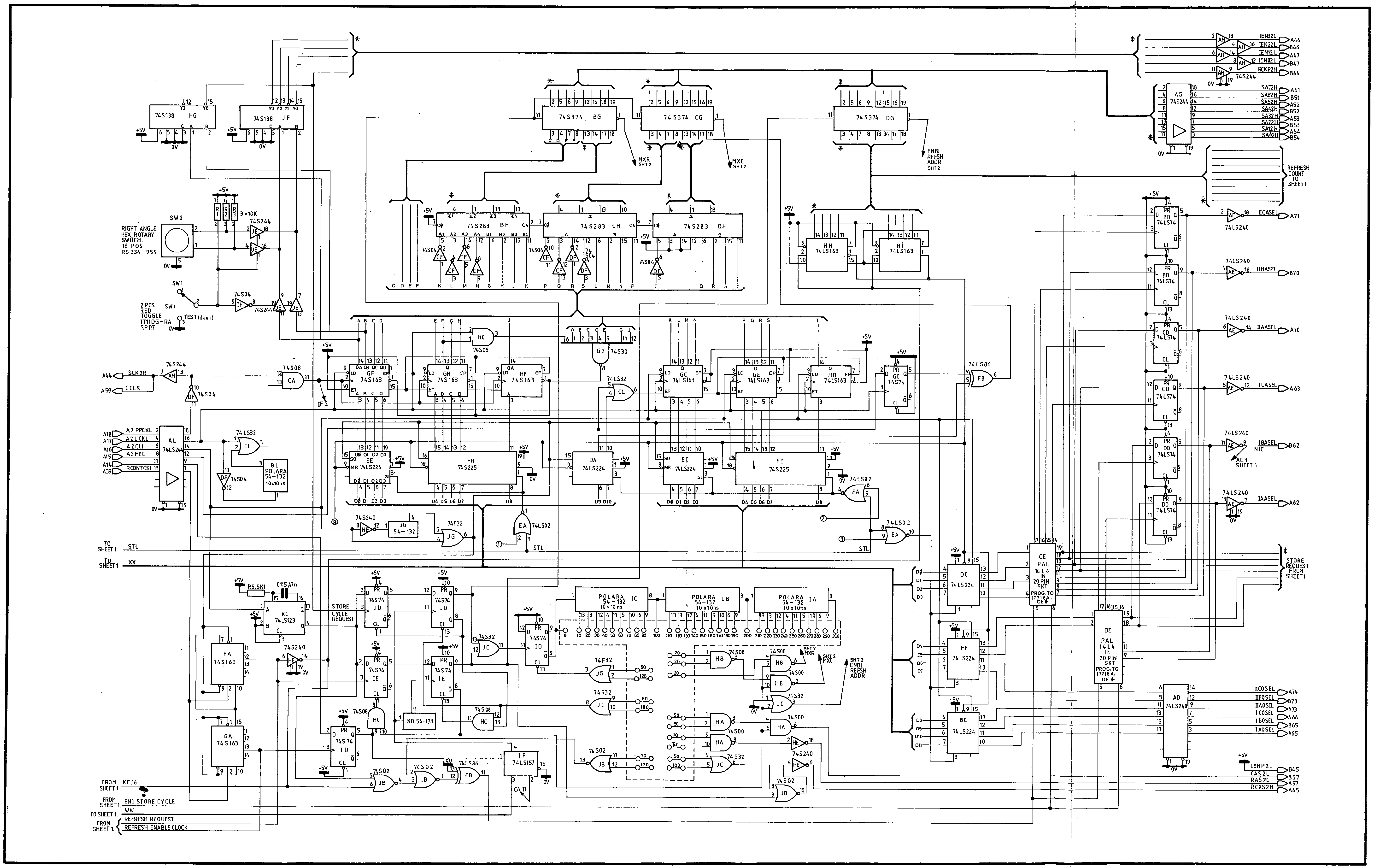
(4,13F)

FIGURE 4.13.3 17716F STORE ADDRESS CIRCUIT 1



(4,13F)

FIGURE 4.13.4 17716F STORE ADDRESS CIRCUIT 2



MUX DEMUX CARD 17717B

4:14:1 Function

The function of each Mux Demux card is to multiplex the data from two satellites (U and V in the bottom rack or Y1 and Y2 in the top rack) when data is read from these Discs, and to de-multiplex the Luminance or U/V when data is to be written into the satellites from the Input Switch card.

4:14:2 Circuit Description

(a) MULTIPLEXED DATA PATH

Data from the Left satellite (Y1 top rack, U bottom rack) is buffered by AF and clocked into the register BF. Data from the Right satellite (Y2 top rack, V bottom rack) is buffered by AE and clocked into the register BE. The registers BF and BE are enabled alternately to provide continuous luminance data (top rack) and multiplexed U/V data (bottom rack).

The data from BF and BE is clocked through the register CE, through the AND gates BC and BD, and passed to the Input Switch card.

The selector DE, the buffer CF and the switch SW3 provide diagnostic facilities which allow the Multiplexed data path to be tested and the satellites to be isolated individually.

(b) DE-MULTIPLEXED DATA PATH

Multiplexed data from the Input Switch card (Y1/Y2 in the top rack and U/V in the bottom rack) is buffered by AI and clocked through the register BI into CI and CH. The inputs of CI and CH are enabled alternately and the data is clocked through to their outputs. The output from CI is clocked through CG and buffered by BG then passed to the Data Select card in the left satellite (Y1 or U). The output from CH is buffered by BH then passed to the Data Select card in the right satellite (Y2 or V).

(c) TIMING CIRCUITRY

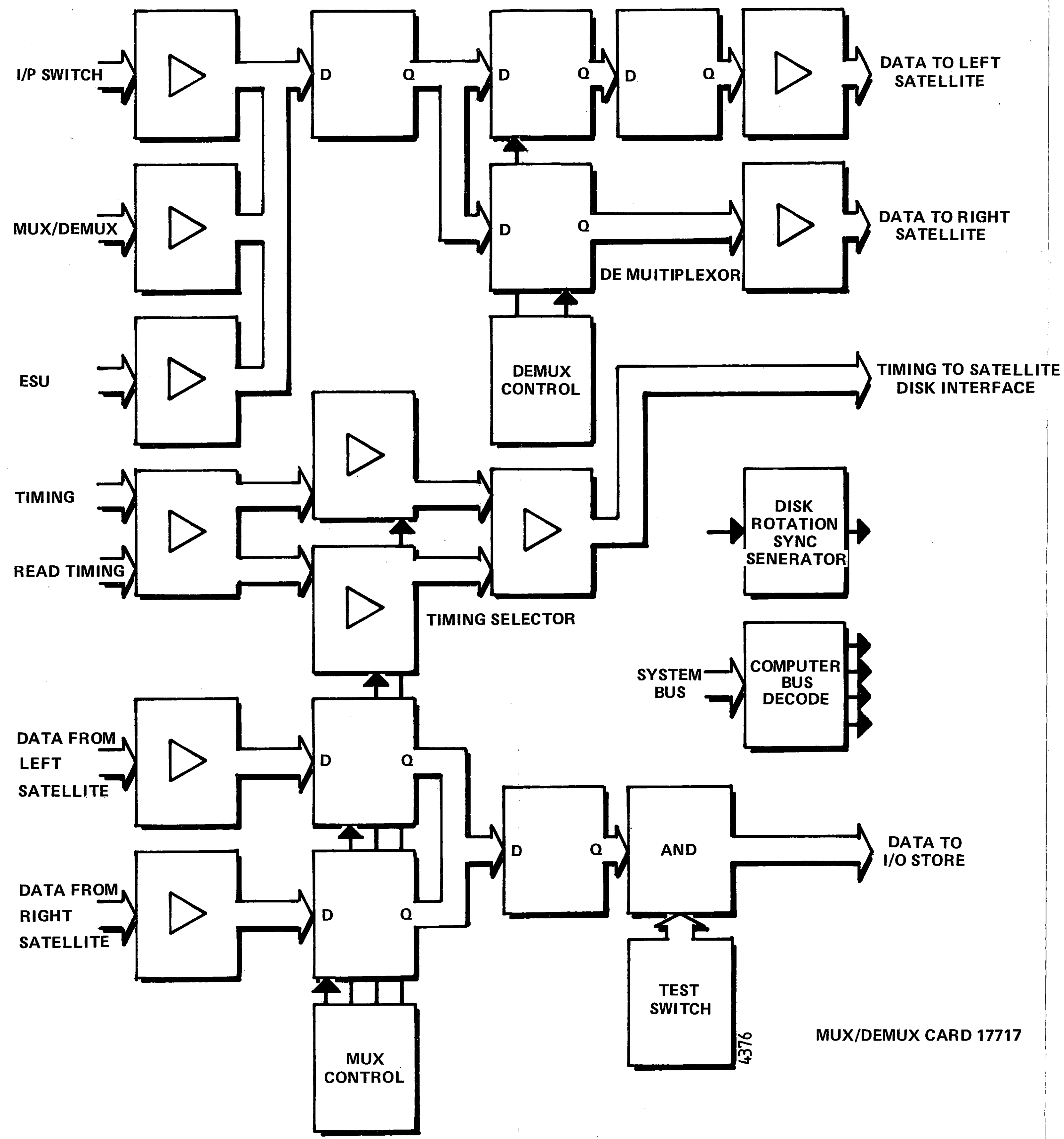
Timing signals from the Input Switch card are buffered by AD and passed to CC and CD, which tri-state select between Read and Write clocks. The Read and Write clocks from CC and CD are then buffered by BB and passed to the two Disc Interface cards.

The counter circuit FE, FF, FG, FH, FI and FB produces the Disc rotational Sync for the two Discs (Y1 and Y2 top rack or U and V bottom rack). This synchronizes the Disc rotation with the system timing.

(d) COMPUTER BUS DECODE

The system computer bus is buffered by AA, AB and AC, and decoded by the Prom BA and the PAL CB to provide the clocks and enables for the computer controlled circuitry on this card.

(4,14B)
FIGURE 4.14.1 17717B MUX DEMUX BLOCK



(4,14B)

FIGURE 4.14.2 17717B MUX DEMUX LAYOUT

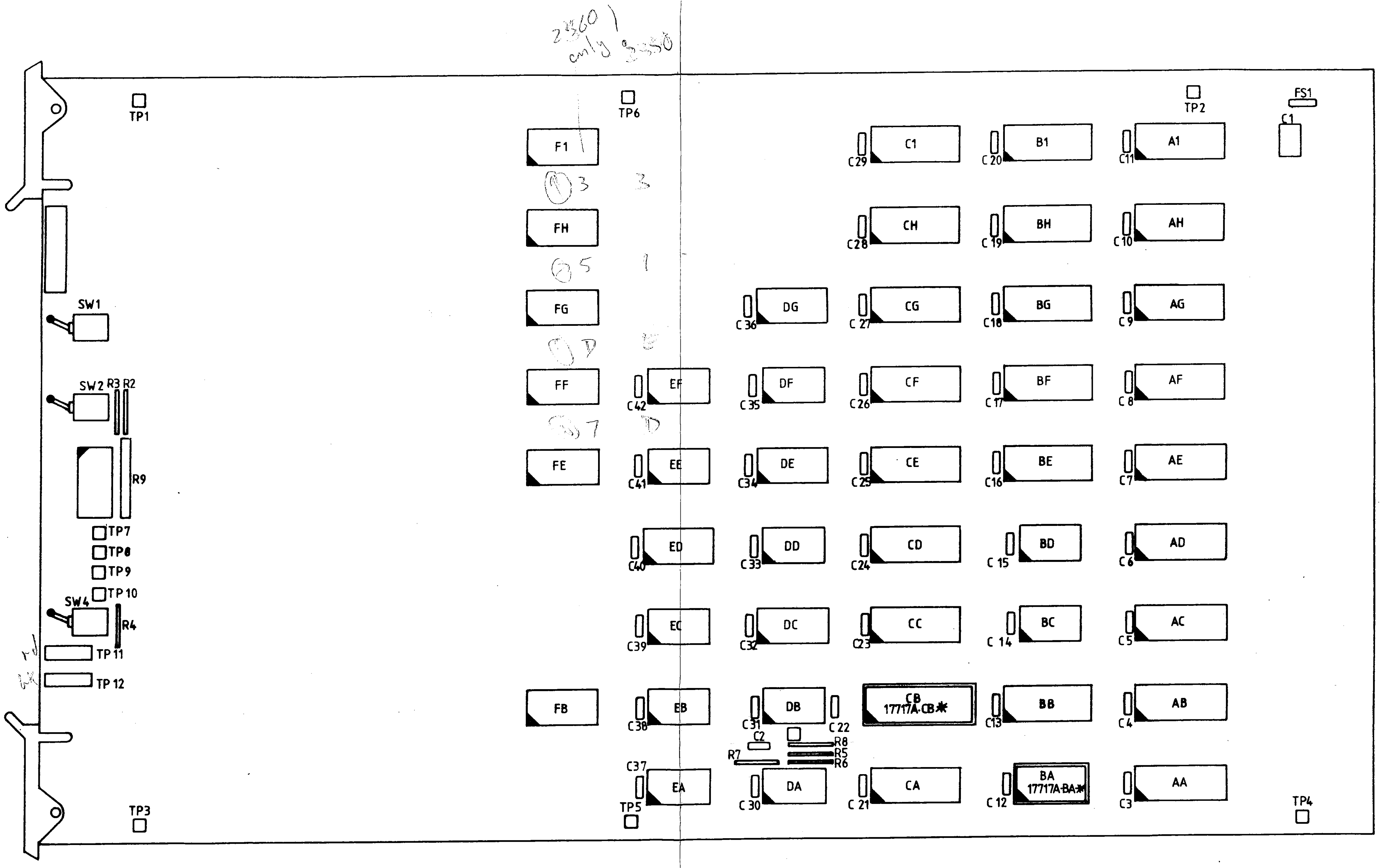
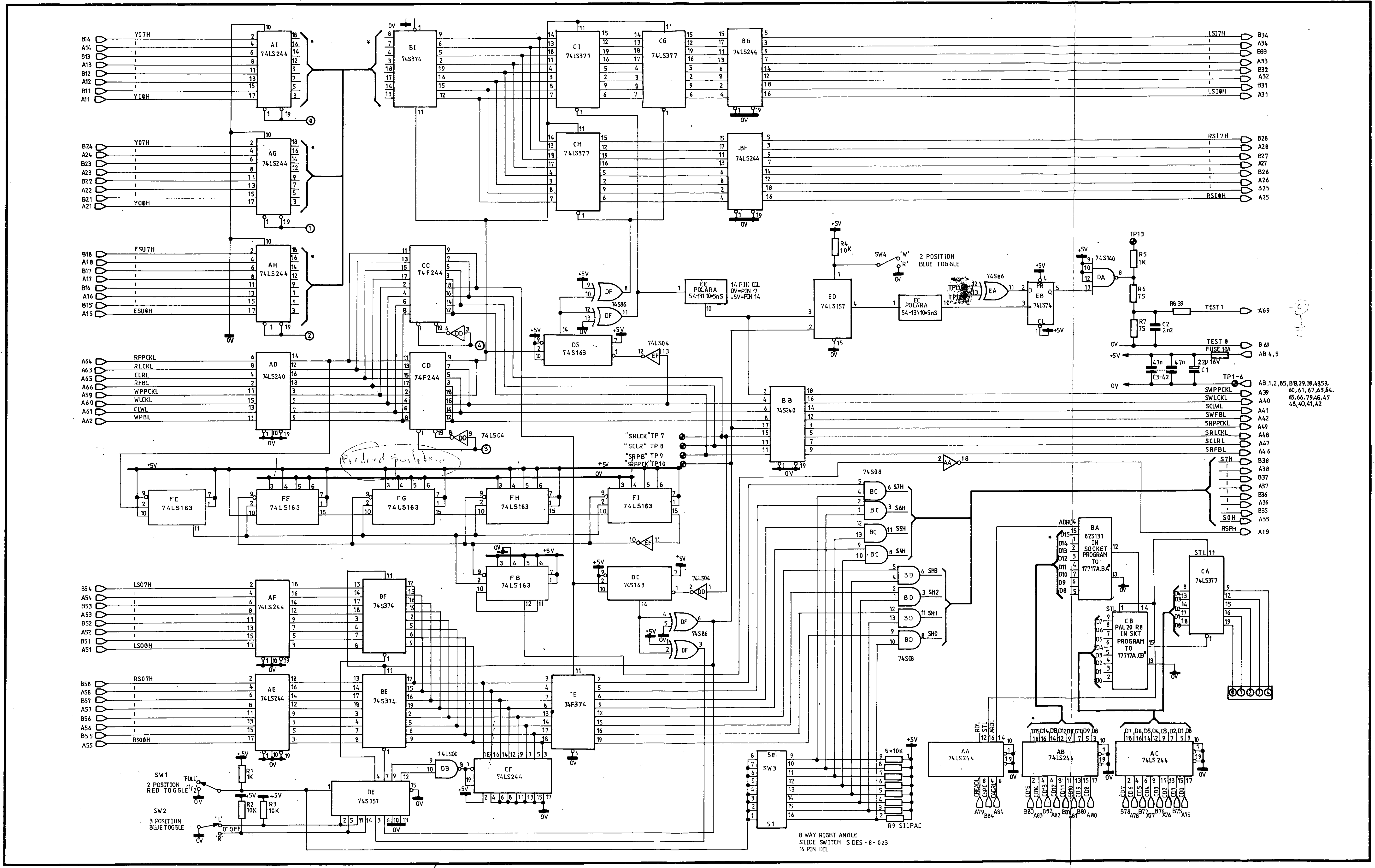


FIGURE 4.14.3 17717B MUX DEMUX CIRCUIT


AI 74LS244
AG 74LS244
AH 74LS244
AD 74LS240
AF 74LS244
AE 74LS244
BI 74S374
BF 74S374
BE 74S374
CI 74LS377
CH 74LS377
CG 74LS377
BG 74LS244
BH 74LS244
CC 74F244
CD 74F244
DG 74S163
DF 74S86
EF 74LS04
DD 74LS04
EE POLARA 54-131 10x5nS
14 PIN DIL 0V=PIN 7 +5V=PIN 14
ED 74LS157
EC POLARA 54-131 10x5nS
EA 74S86
EB 74LS74
DA 74S140
SW4 'W' 'R' 2 POSITION BLUE TOGGLE
TP13
R4 10K
R5 1K
R6 75
R7 75
R8 39
C2 2n2
C1 22µ 16V
C3-42 47n
TEST1 A69
TEST 0 B69
FUSE 10A AB4,5
TP1-6
AB 1,2,B5,B8,29,39,48,59, 60,61,62,63,64, 65,66,79,46,47 48,40,41,42
BB 74S240
"SRLCK" TP 7
"SCLR" TP 8
"SRPB" TP 9
"SRPPCK" TP10
FE 74LS163
FF 74LS163
FG 74LS163
FH 74LS163
FI 74LS163
FB 74LS163
DC 74S163
DF 74S86
74S08
BC
BD
AA
BA 82S131 IN SOCKET PROGRAM TO 17717A.BA
CB PAL20 R8 IN SKT PROGRAM TO 17717A.CB
CA 74LS377
E 74F374
DE 74S157
DB 74LS00
CF 74LS244
AA 74LS244
AB 74LS244
AC 74LS244
SW1 'FULL' 2 POSITION RED TOGGLE 1/2
SW2 3 POSITION BLUE TOGGLE 'L' 'O' OFF 'R'
R1 1K
R2 10K
R3 10K
SW3
8 WAY RIGHT ANGLE SLIDE SWITCH SDES-8-023 16 PIN DIL
8x10K R9 SILPAC
Y17H Y10H Y07H Y00H ESU7H ESU0H
RPPCKL RLCKL CLRL RFBL WPPCKL WLCKL CLWL WPBL
LS07H LS00H RS07H RS00H
LS17H LS10H RSI7H RSI0H
SWPPCKL SWLCKL SCLWL SWFBL SRPPCKL SRLCKL SCLRL SRFBL
S7H S0H RSPH
S7H S6H S5H S4H SH3 SH2 SH1 SH0
CREADL CSPC CADRL RDL STL ARDL
B14 A14 B13 A13 B12 A12 B11 A11
B24 A24 B23 A23 B22 A22 B21 A21
B18 A18 B17 A17 B16 A16 B15 A15
A64 A63 A65 A66 A59 A60 A61 A62
B54 A54 B53 A53 B52 A52 B51 A51
B58 A58 B57 A57 B56 A56 B55 A55
B34 A34 B33 A33 B32 A32 B31 A31
B28 A28 B27 A27 B26 A26 B25 A25
A39 A40 A41 A42 A49 A48 A47 A46
B38 A38 B37 A37 B36 A36 B35 A35 A19
A79 B84 A84 B83 A83 B82 A82 B81 A81 B80 A80
B78 A78 B77 A77 B76 A76 B75 A75

card modified for 2300 | 20cur drives.

INPUT SWITCH CARD 17718D

4:15:1 Function

This card has the following functions; to select Live, Digital or Satellite data for processing; to Interpolate data before it is compressed into the I/O Store; to provide the Menu Cursor.

The Input Switch card also holds a computer timing signal generator circuit, which is used to write the Menu into the I/O Store.

4:15:2 Circuit Description

(a) LUMINANCE DATA PATH

Luminance data from the Chroma Proc card buffered by AJ, from the Codec card buffered by AI, from the Mux Demux card buffered by AH or a computer loaded value from CI is selected and clocked through the register CH. The luminance data, when not Interpolating, is then clocked through the registers BK and AK and passed to the I/O Store and the Mux Demux cards.

(b) LUMINANCE INTERPOLATOR

When the picture is to be compressed, Luminance data from CH is passed to the adder circuit FI, GJ and GH, where delayed Luminance data from the selector circuit FH, GL and FG is added. The output from this adder circuit is clocked through the pipe line register GI into the vertical Interpolator circuit.

Luminance data from GI is passed to the adder circuit CK, CL and FL, where delayed Luminance data from the selector circuit EK, DK and DJ is added. The output from this adder is clocked through the registers BL and EL and written into th RAMs DL, DK and DJ, which provide one line delayed Luminance data. The Interpolated data produced by the adder is clocked through the register AK and passed to the I/O Store.

The counter circuit HJ, EG, EJ and FJ addresses the PAL EH, which controls the Horizontal and Vertical Interpolator circuits to produce an Interpolated data point every 4th picture point on every 3rd line.

(4,15D)

(c) U/V DATA PATH

U/V data from the Chroma Filter card buffered by AG, from the Codec card buffered by AF, from the Mux Demux card buffered by AE or computer loaded values from CF and CG are selected and clocked through the register BF. The U/V data, when not Interpolating, is clocked through the registers DG and BJ and passed to the I/O Store and the Mux Demux cards.

When the picture is Interpolated U/V data from BF is clocked into the two registers DI and DH for each Interpolated Luminance point. Then the U and V data is multiplexed to provide continuous U/V data at the output of BJ.

(d) COMPUTER CLOCK SIGNAL GENERATOR

The horizontal counter circuit DA, EA and DB is clocked by picture point clocks and counts up to FFF from the loaded value held in the computer loaded registers CA and CB. When FFF is reached a horizontal reset signal is produced on HH pin 17.

The vertical counter circuit DC, EC and ED is clocked by the horizontal reset signal and counts up to FFF from the loaded value held in the computer loaded registers CC and DD. When FFF is reached a vertical reset signal (Disk Frame or Video Field) is produced on HH pin 15.

Disk and Video clocks and timing signals are buffered by BE, BB and HH, which form the clock selector circuit. This circuit operates in conjunction with the data selectors so that the appropriate clocks and timing signals are used with the selected video source.

(e) CURSOR GENERATOR

The horizontal counter circuit EB, GB and GA is clocked with picture point clocks and counts up to FFF from the loaded value of horizontal cursor position held in the computer loaded registers FB and FA. The vertical counter circuit GC, GD and GE is clocked with line clocks and counts up to FFF from the loaded value of vertical cursor position held in the computer loaded registers FC and EE.

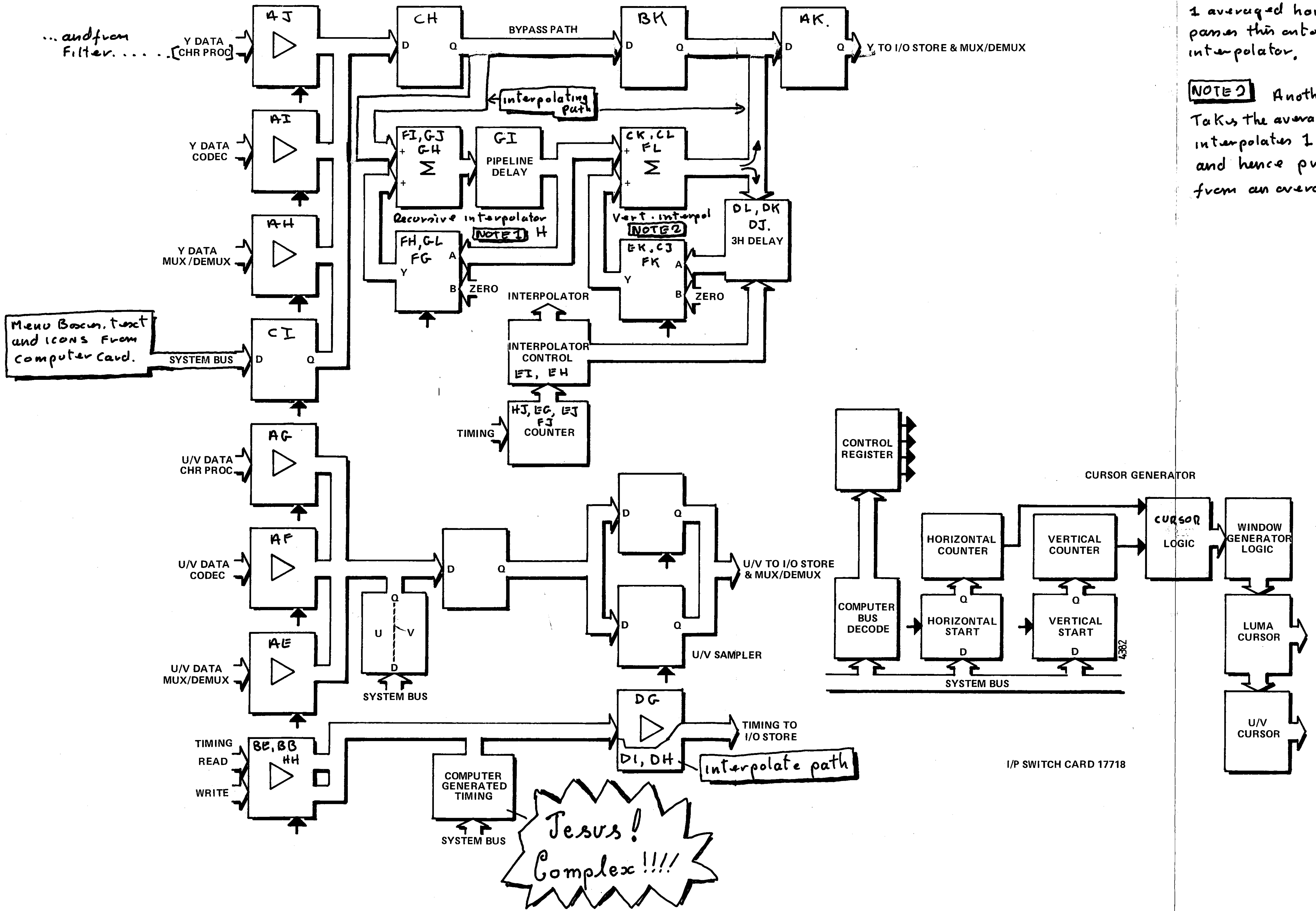
When both counter circuits reach FFF the cursor circuit is enabled by IH. Then the counter circuits IB, IF and HA, IA address the Cursor Shape PAL HB. This produces control signals which enable the register CD (White), the buffer BD (Black) and the registers AC and AD (U and V colour).

(f) COMPUTER BUS DECODE

The system computer bus is buffered by BA, AA and AB, and decoded by the Prom EF and the PALs FE and FD to produces the clocks and enables for the computer controlled circuit on this card. The Control registers FF and DE are loaded with the required function to be performed by the card.

(4,15D)

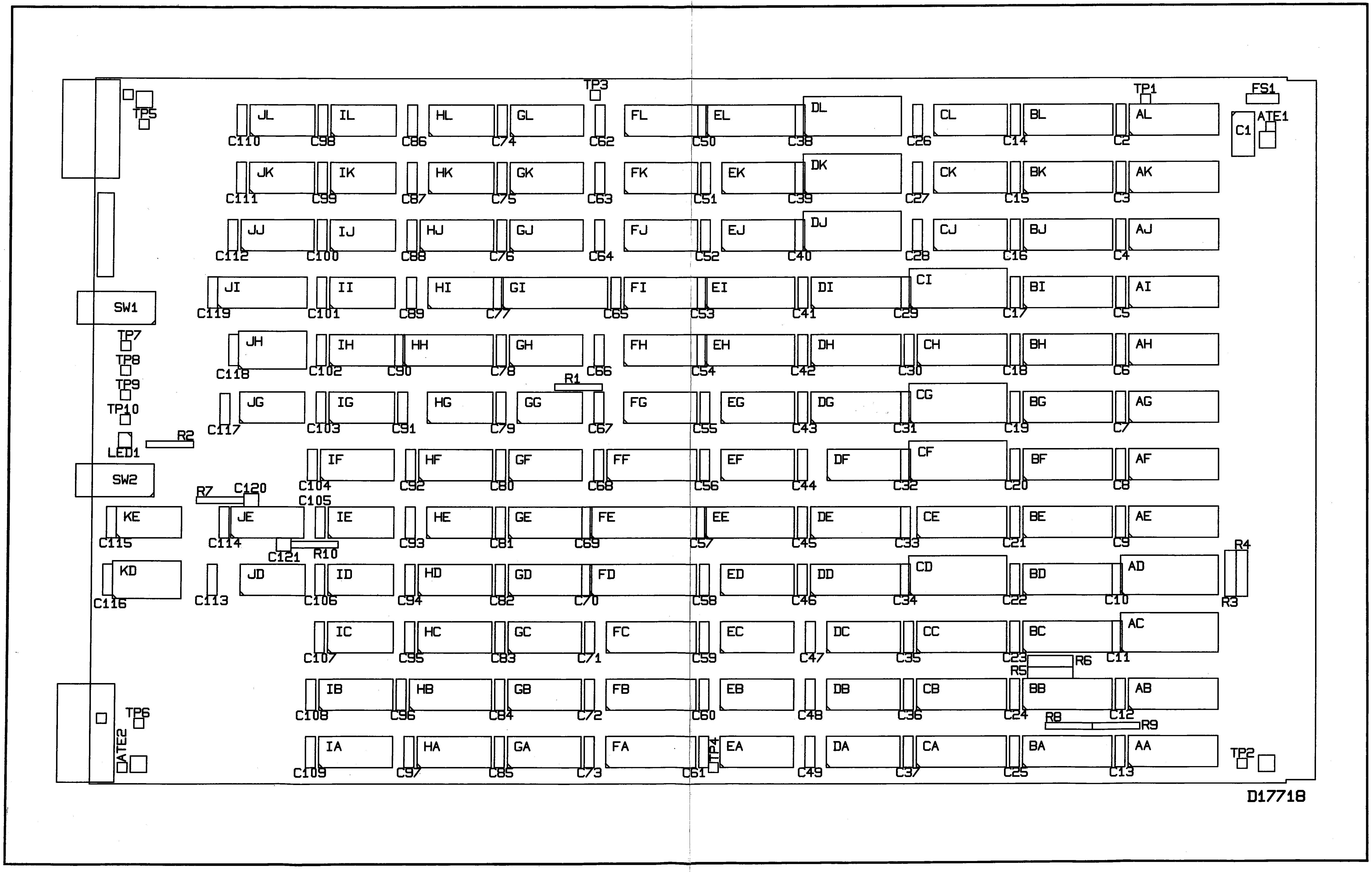
FIGURE 4.15.1 17718D INPUT SWITCH BLOCK



NOTE 1 Recursive interpolator takes 4 real time pixels & makes 1 averaged horizontal pixel & passes this onto the vertial interpolator.

NOTE 2 Another interpolator, Takes the averaged line pixel & interpolates 1 out of 4 of these and hence produces 1 pixel from an overall 16 pixels!!

FIGURE 4.15.2 17718D INPUT SWITCH LAYOUT



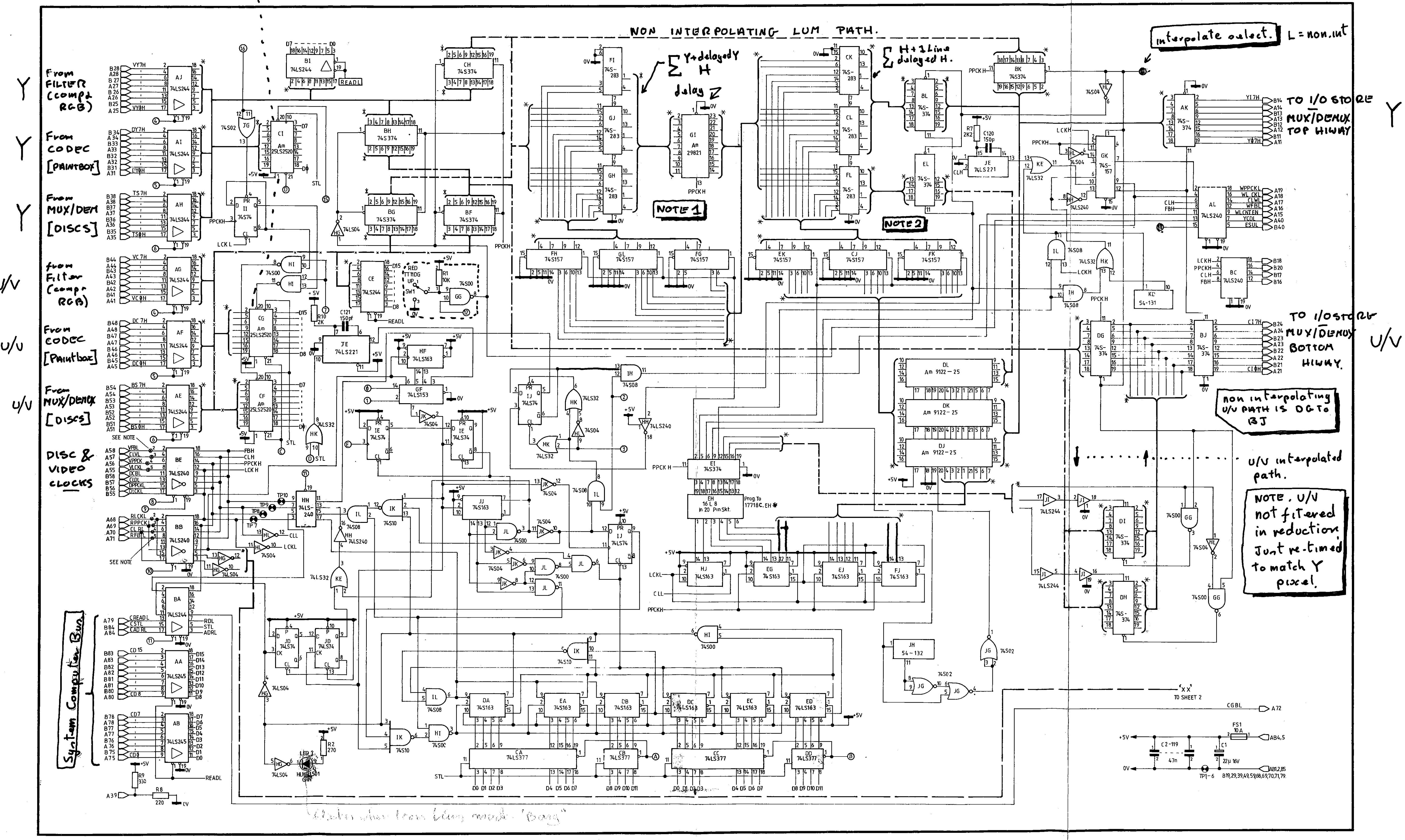
COMPUTER DATA
Menu Boxes &
TEXT.
+ CHROMA.
HI = U/V
Select.

STL = STROBE
RDL WR
RD
ADRL data
ADDR

SW1. SWAP U/V & Y
Powerfull Medicine !!

(4,15D)

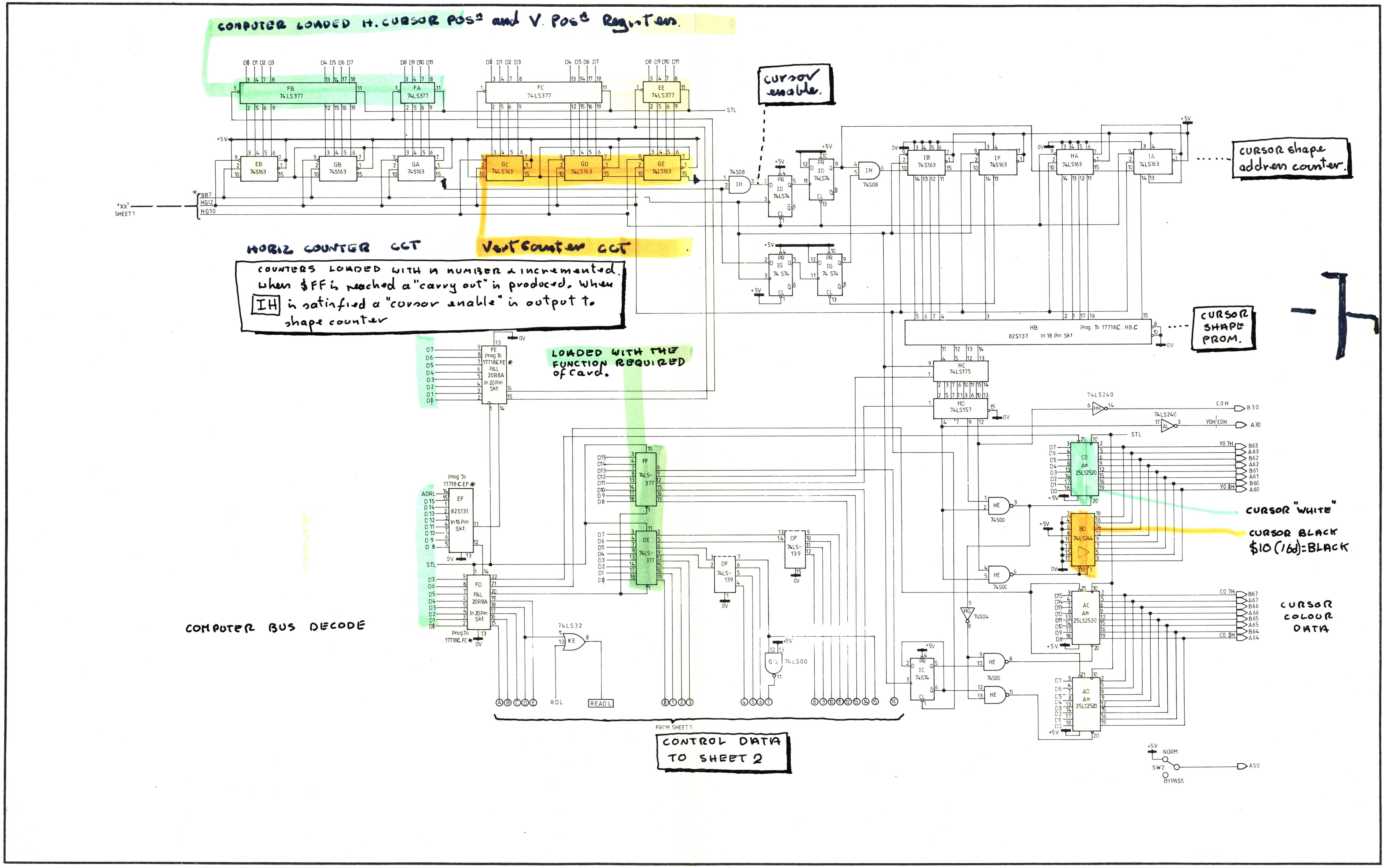
FIGURE 4.15.3 17718D INPUT SWITCH CIRCUIT 1



HORIZONTAL COUNTERS.

VERTICAL COUNTERS.

FIGURE 4.15.4 17718D INPUT SWITCH CIRCUIT 2



COMPUTER LOADED H. CURSOR POSn and V. POSn Registers.

cursor enable.

CURSOR shape address counter.

HORIZ COUNTER CCT

Vert Counter CCT

COUNTERS LOADED WITH A NUMBER & incremented. when $FF is reached a "carry out" is produced. When IH is satisfied a "cursor enable" is output to shape counter

CURSOR SHAPE PROM.

LOADED WITH THE FUNCTION REQUIRED of card.

CURSOR "WHITE"

CURSOR BLACK $10 (16d) = BLACK

CURSOR COLOUR DATA

COMPUTER BUS DECODE

CONTROL DATA TO SHEET 2

cursor changes colour dependant on which operation is to be performed & is injected directly into o/p processor "picture", full frame, cells etc has been loaded into I/O STORE.

I/O STORE CONTROL CARD 17720D

4:16:1 Function

The function of this card is to produce the addresses, strobes and enable signals for the I/O Store. This card has two similar address generator circuits which produce independent Read and Write addresses which enable synchronous Read and Write cycles to be performed.

4:16:2 Circuit Description

(a) WRITE ADDRESS GENERATOR

The horizontal counter circuit GJ, GI and IG is clocked by picture point clocks and counts up from the loaded value held in the computer loaded registers HI and II. The 4-bit count from GJ is passed to the decoders CH and DM which produce 12 stripe enable signals. These are buffered by AI and AJ and passed to the I/O Store.

The 4-bit count from GJ is also passed to FK, EK, FL and EL, which produce 12 write enable signals. These are clocked through the registers FJ, EJ, FI and EI then passed to the I/O Store cards via the AND gates AH, BG and BH. The 6-bit count from GI and IG is clocked through the register AM, which forms part of the RAS/CAS address multiplexer circuit.

The vertical counter circuit EM, BM and FM is clocked by line clocks and counts up from the loaded value held in the computer loaded registers GM and IE. The 9-bit count produced is clocked through the registers AL and AM which form part of the RAS/CAS address multiplexer circuit.

The RAS/CAS address multiplexer circuit is controlled by the decoder BL which enables Read or Write RAS/CAS addresses on to the address bus, determined by the store control circuit. The address bus is buffered by AG and passed to the I/O Store cards.

(b) CROP CIRCUITRY

The horizontal count from GJ, GI and IG is passed to the comparator circuit HJ, IJ and ID, where the count is compared with the horizontal crop position and length values held in the computer loaded FIFOs HH, IK and IF. When the count reaches the crop position value the AND gate CL produces a flag that is passed to the Crop circuit IC, IB and GA. This action selects the crop length value from the FIFOs and produces a write enable signal. When the crop length value is reached, the crop circuit disables the write enable signal.

The vertical count from EM, BM and FM is passed to the comparator circuit IL, HL and GL, where the count is compared with the vertical crop position and length values held in the computer loaded FIFOs IM, HM and GK. When the count reaches the crop position value a flag is passed to the Crop circuit IC, IB and GA. This action selects the crop length value from the FIFOs and produces a write enable signal. When the crop length value is reached, the crop circuit disables the write enable signal.

When the horizontal and vertical write enable signals coincide, a window is produced which allows data to be written into the selected part of the I/O Store.

(c) STORE CONTROL CIRCUITRY

The store cycle pulse from DK is passed down the delay lines CK, CJ and CI to provide various delayed pulses. These pulses are combined by the logic CH, CG, DE, BI and DK to produce the strobe and control signals for the address multiplexer circuit and for the Dynamic RAMs on the I/O Store cards. The logic CD, CC and CD controls the synchronizing of Read and Write store cycles of the I/O Store.

(d) READ ADDRESS GENERATION

The horizontal counter circuit BB, EB and FB is clocked by picture point clocks and counts up from the loaded value held in the computer loaded registers HB and FA. The 4-bit count from BB is passed to the decoders BC and BD which produce 12 stripe enable signals. These are buffered by AD and AE and passed to the I/O Store. The 6-bit count from EB and FB is clocked through the register BF, which forms part of the RAS/CAS address multiplexer circuit.

The vertical counter circuit HG, HH and IH is clocked by line clocks and counts up from the loaded value. The 9-bit count produced is buffered by GE, GD and GF, GE and passed to the address inputs of the RAMs FE, FD, FC and FF, FG, FH. These RAMs hold computer loaded tables which convert the 9-bit count into a scrolled address count. The output address produced by these RAMs is clocked through the registers EE and EF and passed to the registers BF and BE, which form part of the RAS/CAS address multiplexer circuit.

(e) COMPUTER BUS DECODE

The system computer bus is buffered by AF, AA and AB, then decoded by the Prom BA, the PAL AC and the Proms GG and GH to produce the clocks and enables signals for the computer controlled circuitry on this card.

The RAMs FE, FD, FC and FF, FG, FH are loaded with the appropriate address transformation from the system computer via the buffers ED and EG. The RAM location to be written is addressed from the system computer via the registers HC, HD and HF, HE. The write enable signals for these RAMs are generated by the Proms GG and GH.

(4,16D)
FIGURE 4.16.1 17720D I/O STORE CONTROL BLOCK

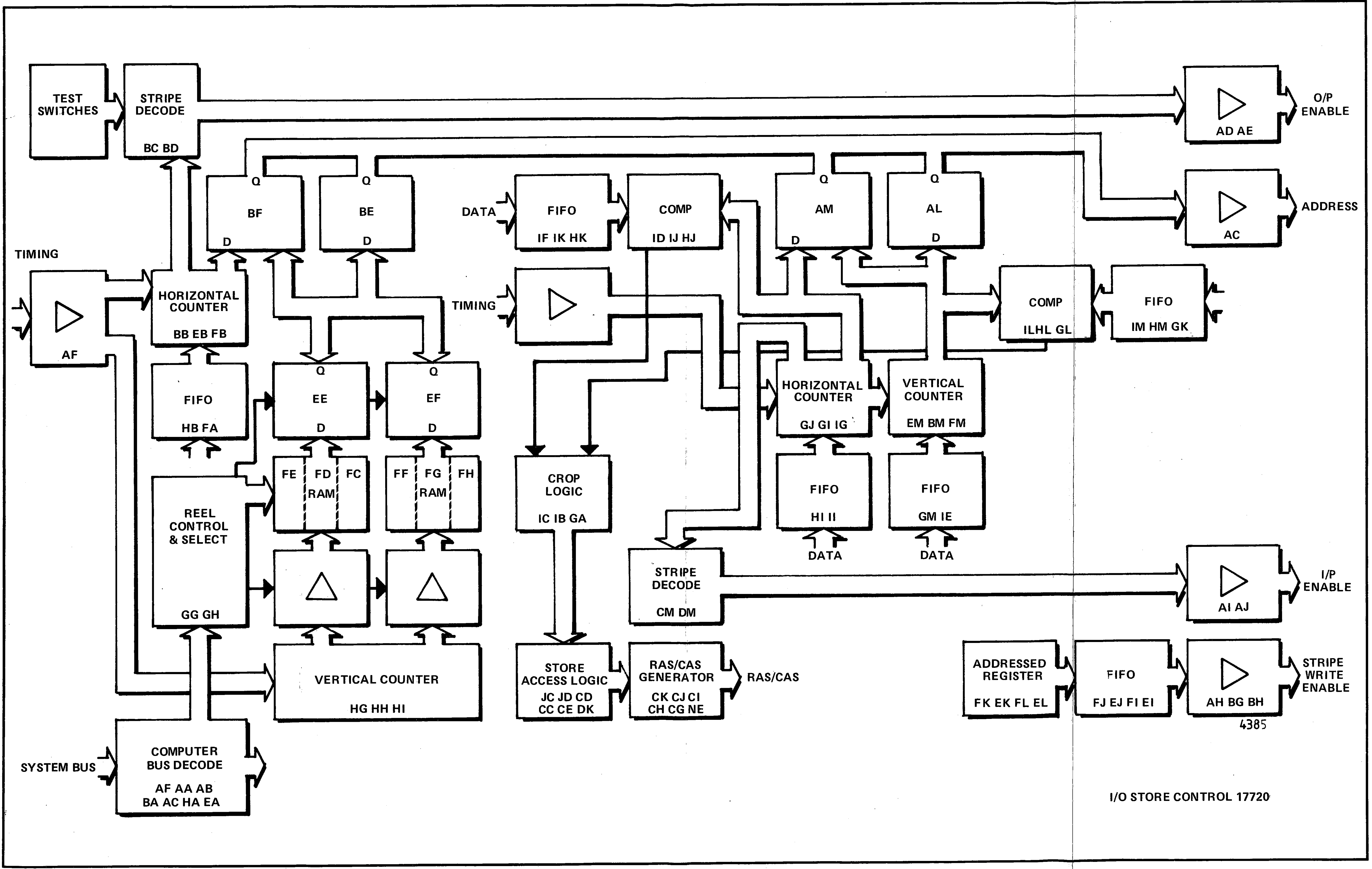
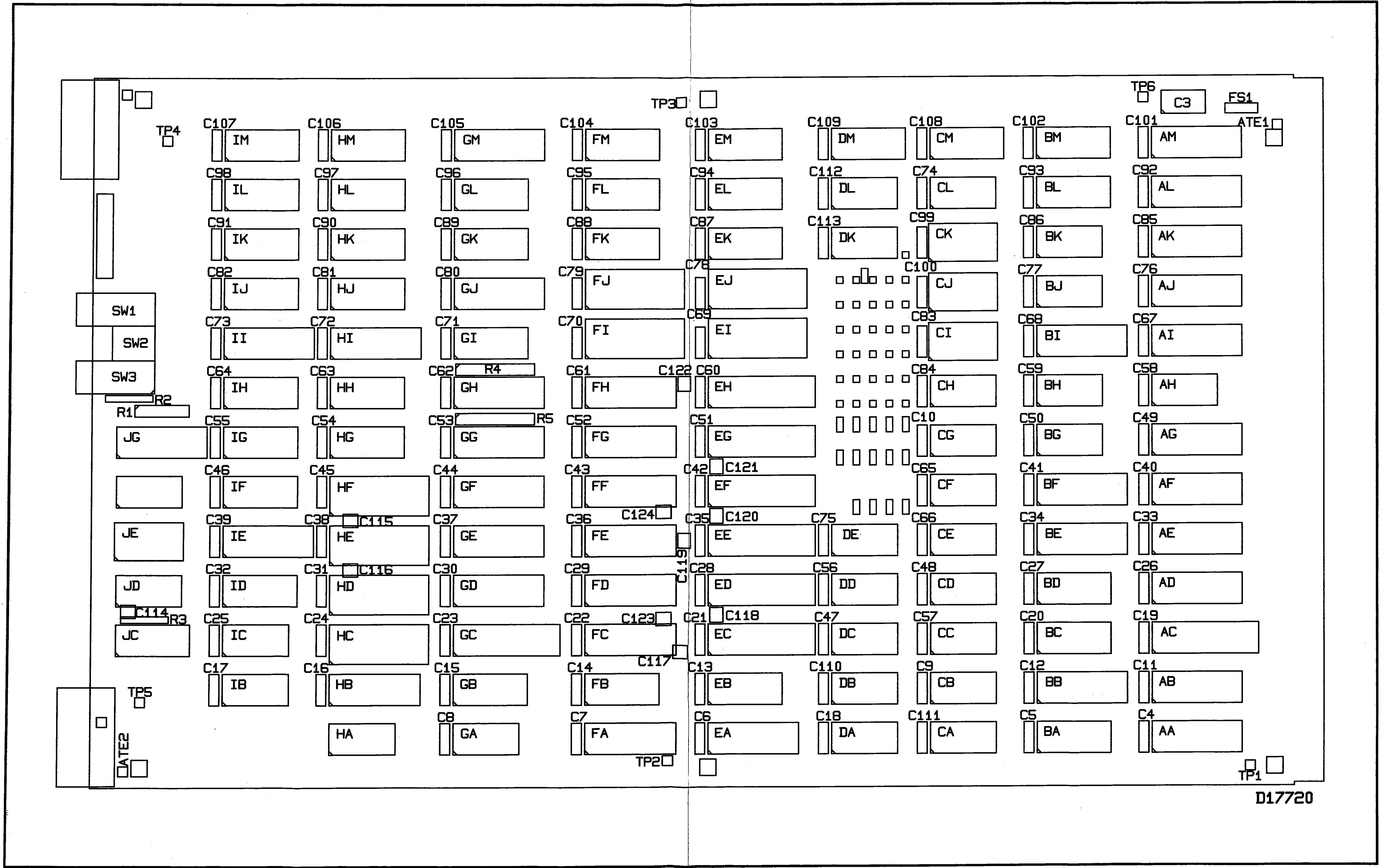
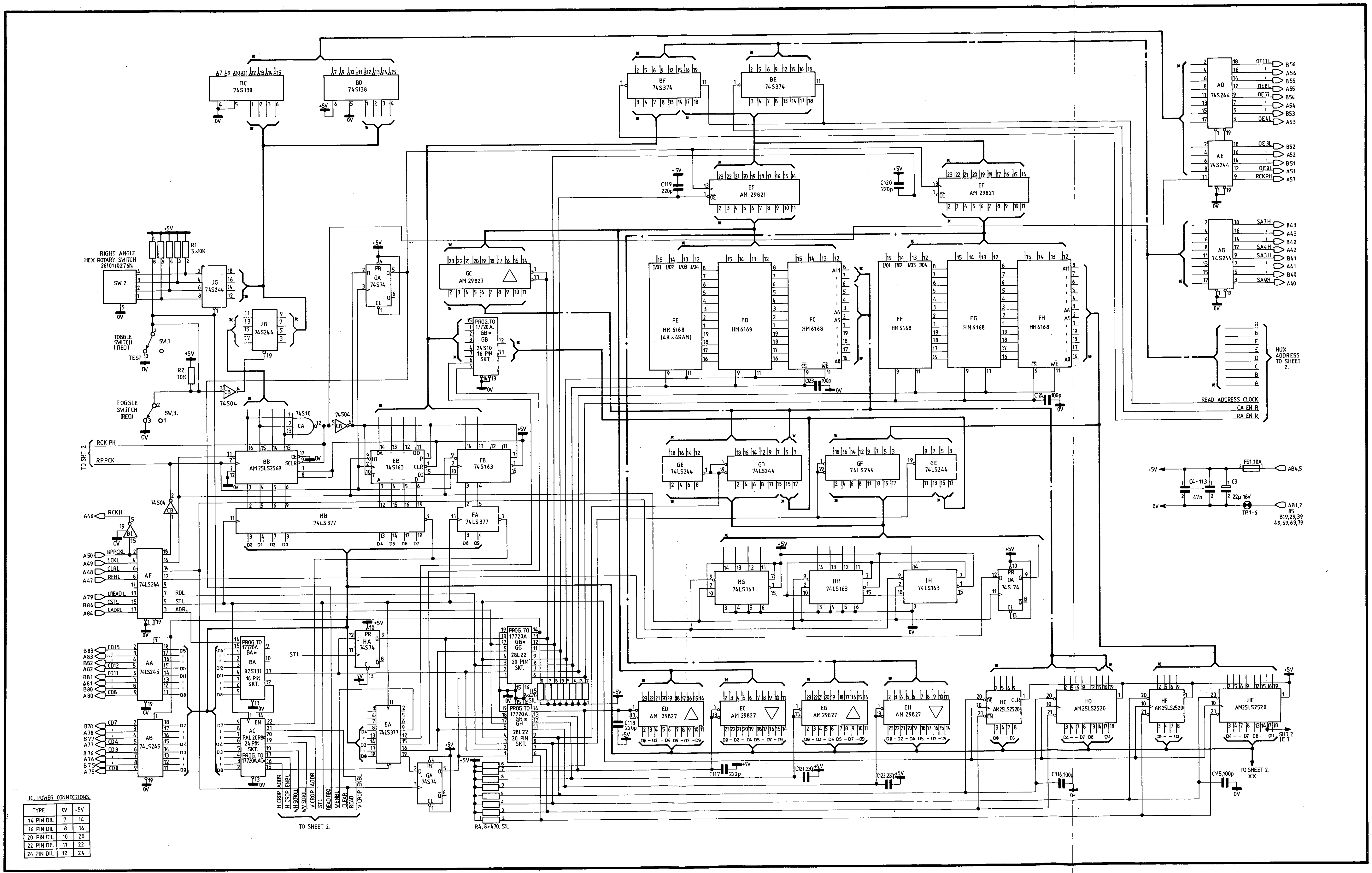


FIGURE 4.16.2 17720D I/O STORE CONTROL LAYOUT



(4,16D)

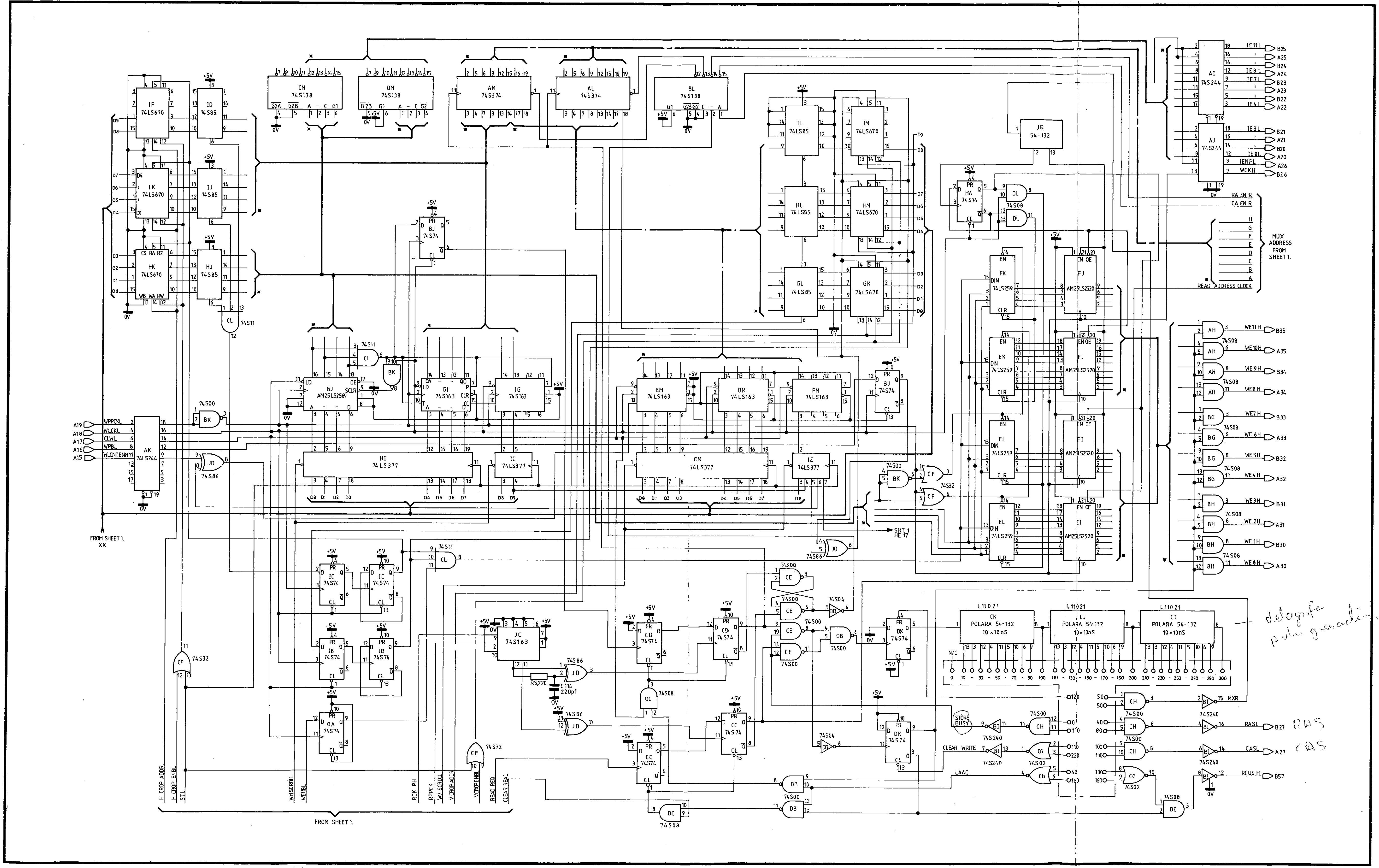
FIGURE 4.16.3 17720D I/O STORE CONTROL CIRCUIT 1



IC. POWER CONNECTIONS.

TYPE	0V	+5V
14 PIN DIL	7	14
16 PIN DIL	8	16
20 PIN DIL	10	20
22 PIN DIL	11	22
24 PIN DIL	12	24

(4,16D)
FIGURE 4.16.4 17720D I/O STORE CONTROL CIRCUIT 2



delay for pulse generation

RAS

CAS

CODEC CARD 2003732A

4:17:1 Function

The function of this card is to provide the video data interface between the Harry and the Paintbox systems. This card provides Luminance and U/V data paths to and from the Paintbox and two sets of Horizontal and Vertical counters which time the Paintbox system to the Harry output reference video.

4:17:2 Circuit Description

(a) VIDEO DATA PATH FROM PAINTBOX

Luminance data from the Paintbox system (via the "INPUT A" socket) is buffered by BH and clocked through the register CH into the PAL DH, which limits the digital range of the data. The data from DH is clocked through the register EH, buffered by FH and then passed to the Input Switch card.

Multiplexed U/V data from the Paintbox system (via the "INPUT A" socket) is buffered by BG and clocked through the register CG into the PAL DG, which limits the digital range of the data. The data from DG is clocked through the register EG, buffered by FG and then passed to the Input Switch card.

(b) VIDEO DATA PATH TO PAINTBOX

Luminance data from the I/O Store is buffered by BD and clocked through the register CD into the PAL DD, which limits the digital range of the data. The data from DD is clocked through the register ED, buffered by FD and passed to the Paintbox via the "OUTPUT A" socket.

Multiplexed U/V data from the I/O Store is buffered by AC and clocked through the register BC into the PAL CC, which limits the digital range of the data. The data from CC is clocked through the register DC, buffered by EC and passed to the Paintbox via the "OUTPUT A" socket.

(c) HORIZONTAL TIMING

The horizontal timing signal RLCKL from the Output Timing card loads the horizontal counter circuit HF, HG and HH with the value held in the computer loaded registers IF and IG. The counter circuit counts up until FFF is reached, and the carry output from HF is clocked through GD to provide the delayed Write side horizontal timing signal PBWRST for the Paintbox system.

The counter circuit KF, KG and IH is loaded with the value held in the computer loaded registers JF and JG to delay the Read side horizontal timing signal PBRLRST from the Paintbox system.

(4,17A)

(d) VERTICAL TIMING

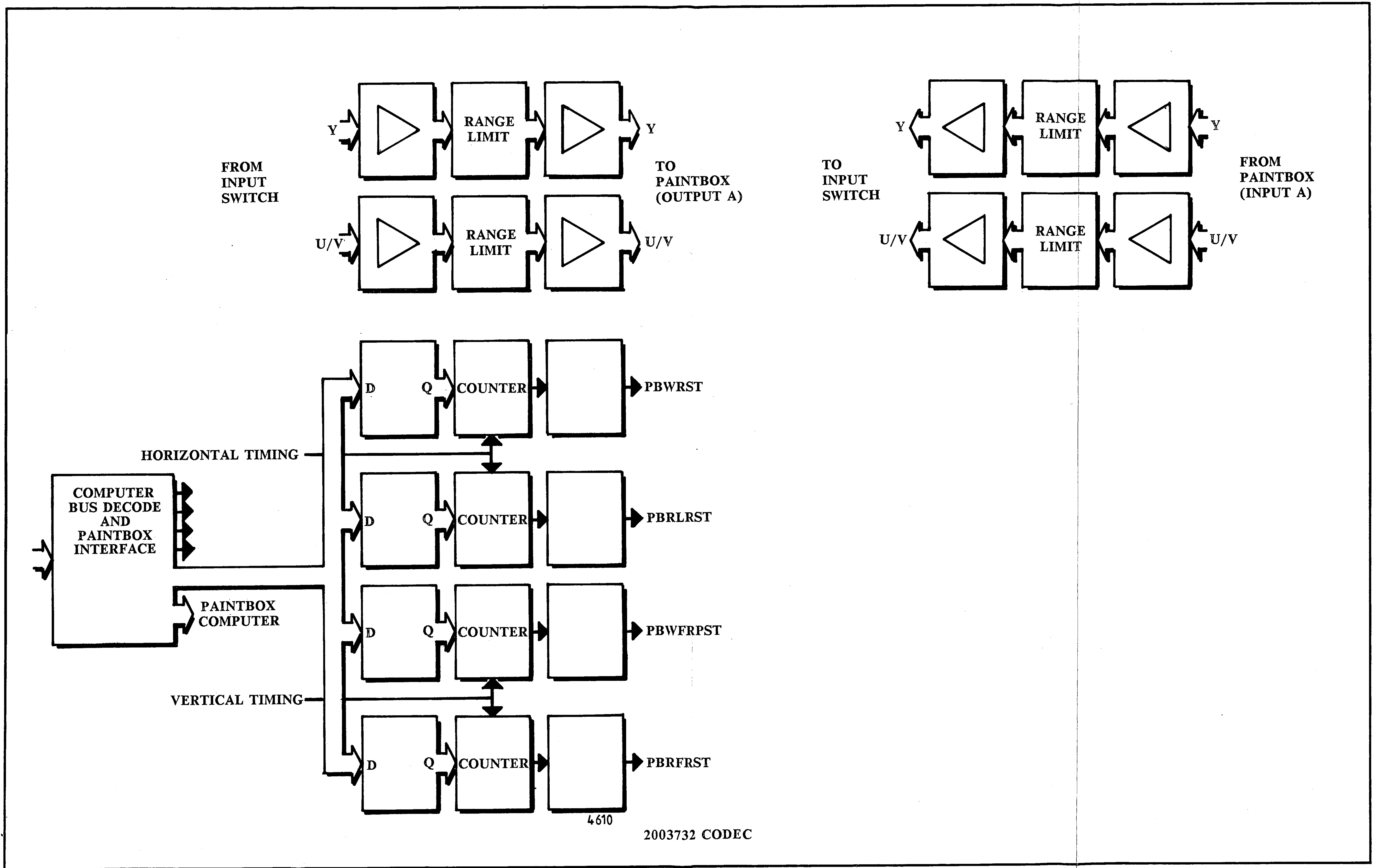
The vertical timing signal CLRL from the Output Timing card loads the vertical counter circuit HD, HC and HA with the value held in the computer loaded registers IA and ID. The counter circuit counts up until FFF is reached, and the carry output from HA is clocked through GD to provide the delayed Write side vertical timing signal PBWRPST for the Paintbox system.

The counter circuit KD, KC and JA is loaded with the value held in the computer loaded registers JA and JD to delay the Read side vertical timing signal PBRFRST from the Paintbox system.

(e) COMPUTER BUS DECODE

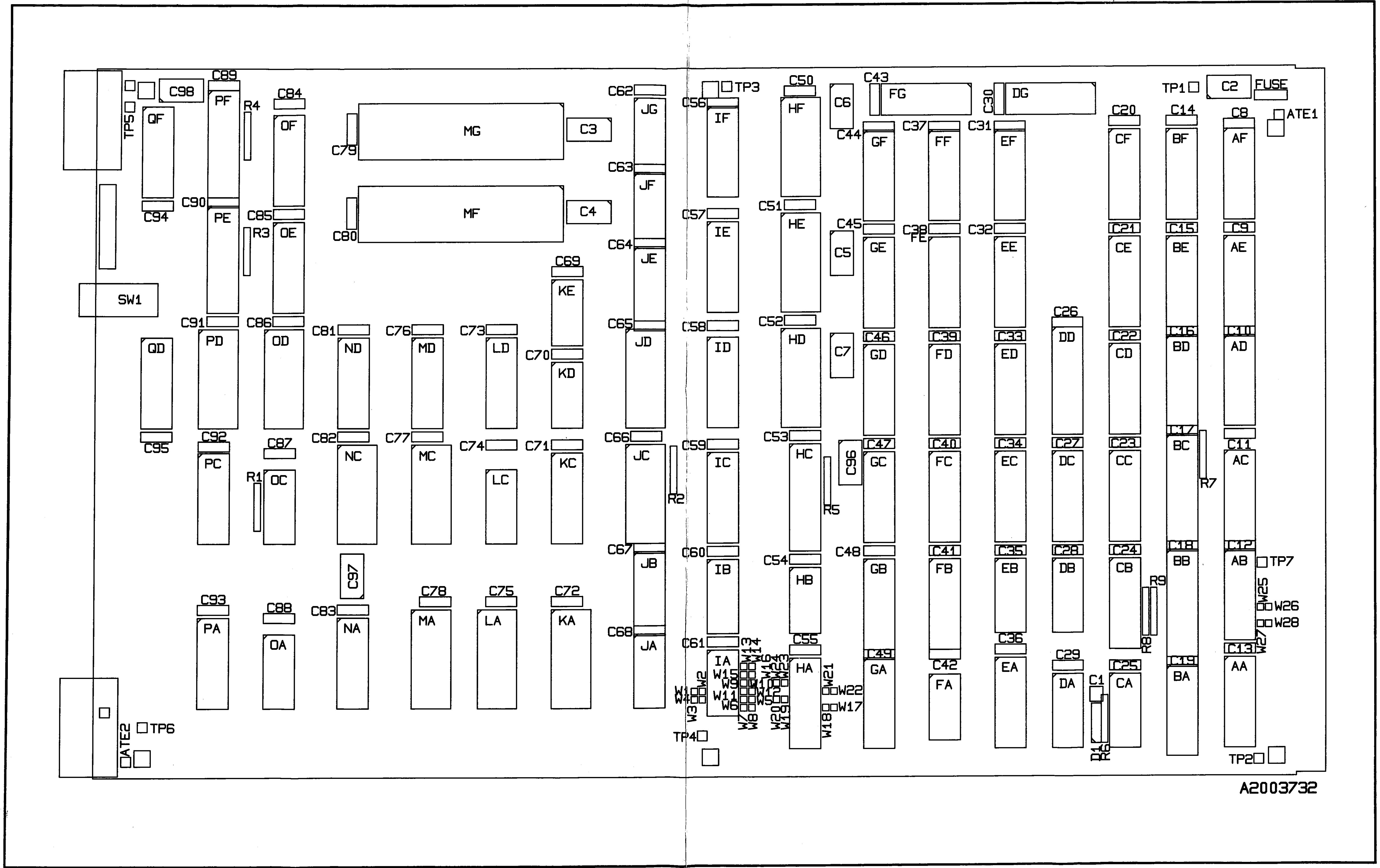
The system computer bus is buffered by AA and CA, and decoded by the Prom BA and the PAL DA, to provide clock and enable signals for the computer controlled circuitry on the card. This computer interface also provides a computer communication path between the Harry and Paintbox systems.

(4,17A)
FIGURE 4.17.1 2003732A CODEC BLOCK



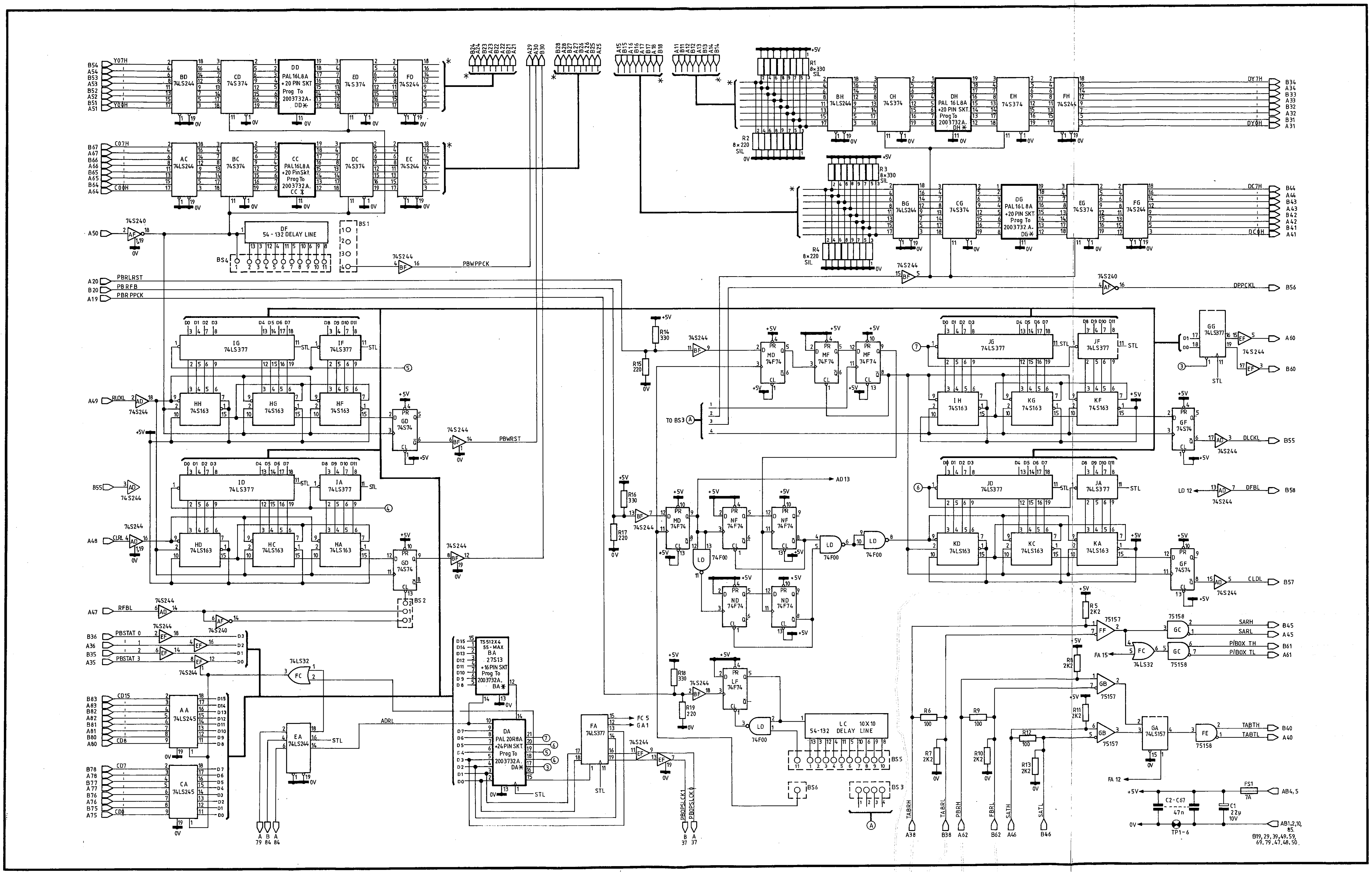
(4,17A)

FIGURE 4.17.2 2003732A CODEC LAYOUT



(4,17A)

FIGURE 4.17.3 2003732A CODEC CIRCUIT



RGB OUTPUT CARD 17723C

4:18:1 Function

The function of this card is matrix the YUV output data to produce RGB data. This data is converted to analogue, filtered, and passed from this card as the RGB output video signals.

This card can also be configured to provide YUV output signals. Normally this card will be configured as RGB or YUV outputs only.

4:18:2 Circuit Description

(a) LUMINANCE DATA PATH

Luminance data from the I/O Store is buffered by BC and clocked through the pipe line register EC into the $\sin^2$ blanking proms FC and GC. These proms produce a $\sin^2$ blanking edge to the Luminance data, when the positive and negative edges of the R BLANK signal occur on A43. The counter CF counts up and down through the 8 states in all the $\sin^2$ blanking proms, which changes the amplitude of the data passing through them.

The blanked Luminance data is clocked through the registers HC and IC into the Red, Green and Blue matrix circuits.

(b) U/V DATA PATH

Multiplexed U/V data from the I/O Store is buffered by AC and passed to the de-multiplexer and interpolator circuit. U and V data from AC is clocked through the registers BD and BE (which provides delayed U and V data), into the adder circuit CD and BF. This adder produces alternate samples of interpolated U and V data. This interpolated data is passed to the data selector circuits DE and DF (for V data), and CE and EF (for U data), where selection between normal and interpolated data is made on alternate samples.

The continuous V and U data produced is passed to the $\sin^2$ blanking proms GF and FE, which produces $\sin^2$ blanking edges to the data, when a positive or negative edge occurs on the R BLANK signal.

The blanked V and U data produced is clocked through the registers HF and GE into the scaling proms KF, IF and HF (for V data), and IE, HE and KE (for U data). The scaled data from these proms is registered and passed to the Red , Green and Blue matrices.

(c) GREEN OUTPUT

Luminance data from IC is passed to the adder circuit LD, KD and JD, where scaled V data from LF and JF is added. The output from this adder is passed to the adder circuit LC, KC and JC, where scaled U data from JE and JF is added. The output from this adder is passed to the adder circuit MC, NB and NC, where shaped sync data from NA is added.

The prom OA produces a shaped sync pulse edge, when a positive or negative edge occurs on the R SYNC signal on A42. The counter LA counts up and down through the 8 states in the OA, which produces the values for the sync pulse.

The Y plus syncs or Green plus syncs data from the adder MC, NB and NC is clocked through the registers MB and OC, through the PAL PC into the DAC QC. The output from this DAC is filtered by FLT 1, buffered and amplified by the discrete amplifier circuit TR1, TR2 and TR3, then outputted as the Green or Y output signal.

(d) RED OUTPUT

Luminance data from IC is passed through the "RGB/YUV" selector circuit ID and HD into the adder circuit OE, OD and ME, where scaled V data from NF and JF is added. The Red or V data produced is passed through the PAL OF, and clocked through the register PF into the DAC QF. The output from this DAC is filtered by FLT 2, buffered and amplified by the discrete amplifier circuit TR4, TR5 and TR6, then outputted as the Red or V output signal.

(e) BLUE OUTPUT

The Luminance data from the "RGB/YUV" selector circuit ID and HD is passed to the adder circuit ND, MD and NE, where scaled U data from LE and JF is added. The Blue or U data produced is passed through the PAL PD, and clocked through the register PE into the DAC QE. The output from this DAC is filtered by FLT 3, buffered and amplified by the discrete amplifier circuit TR7, TR8 and TR9, then outputted as the Blue or U output signal.

(f) COMPUTER BUS DECODE

The bottom 8 bits of the computer bus, and the control strobes are decoded by the PAL FA to produce the appropriate clocks and enables for the computer controlled circuitry on this card.

4:18:3 Presets

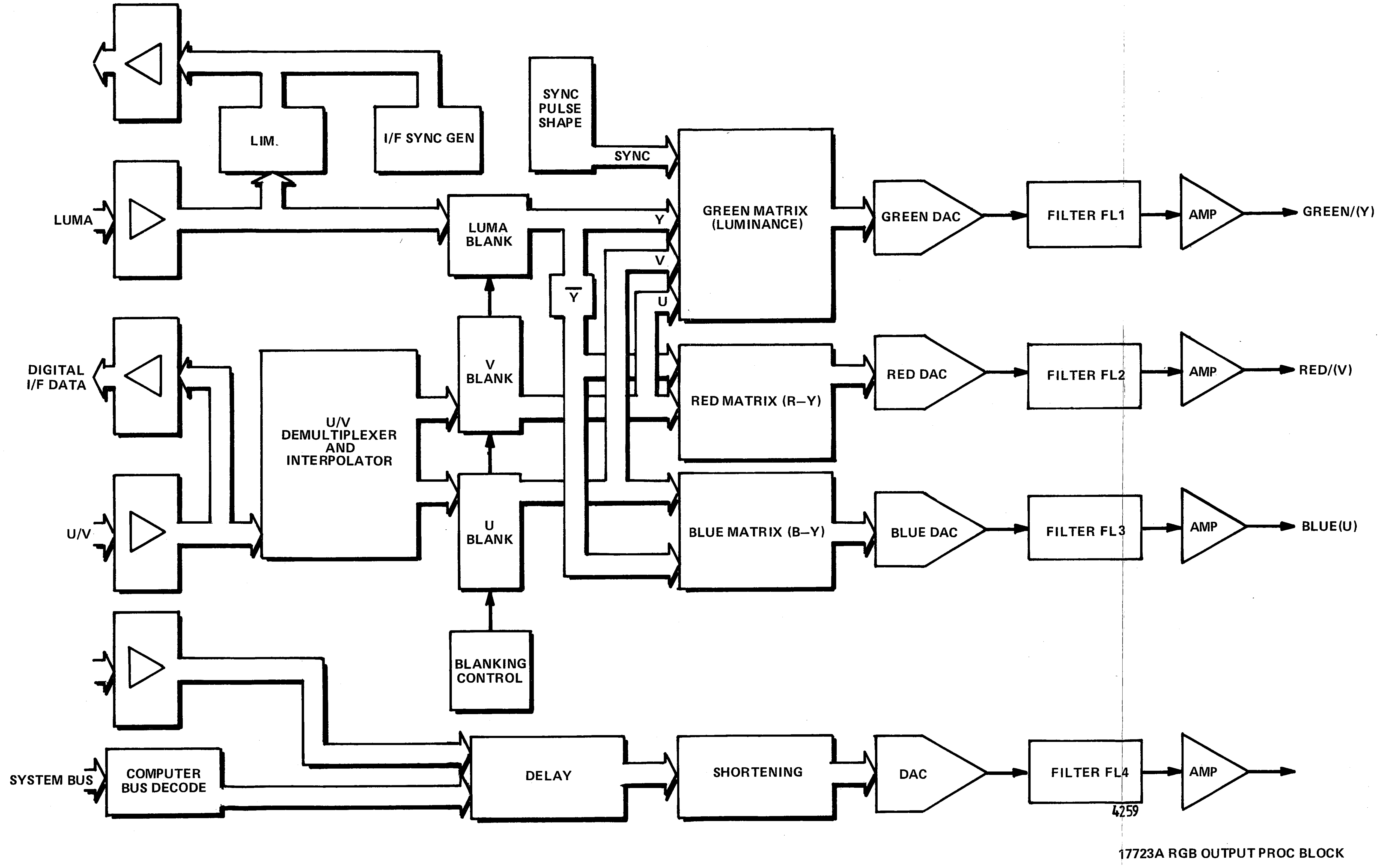
(a) VR1 Red balance adjustment

(b) VR2 Output Amplitude adjustment

(c) VR3 (Not used)

(d) VR4 Blue balance adjustment

(4,18C)
FIGURE 4.18.1 17723C RGB OUTPUT BLOCK



(4,18C)

FIGURE 4.18.2 17723C RGB OUTPUT LAYOUT

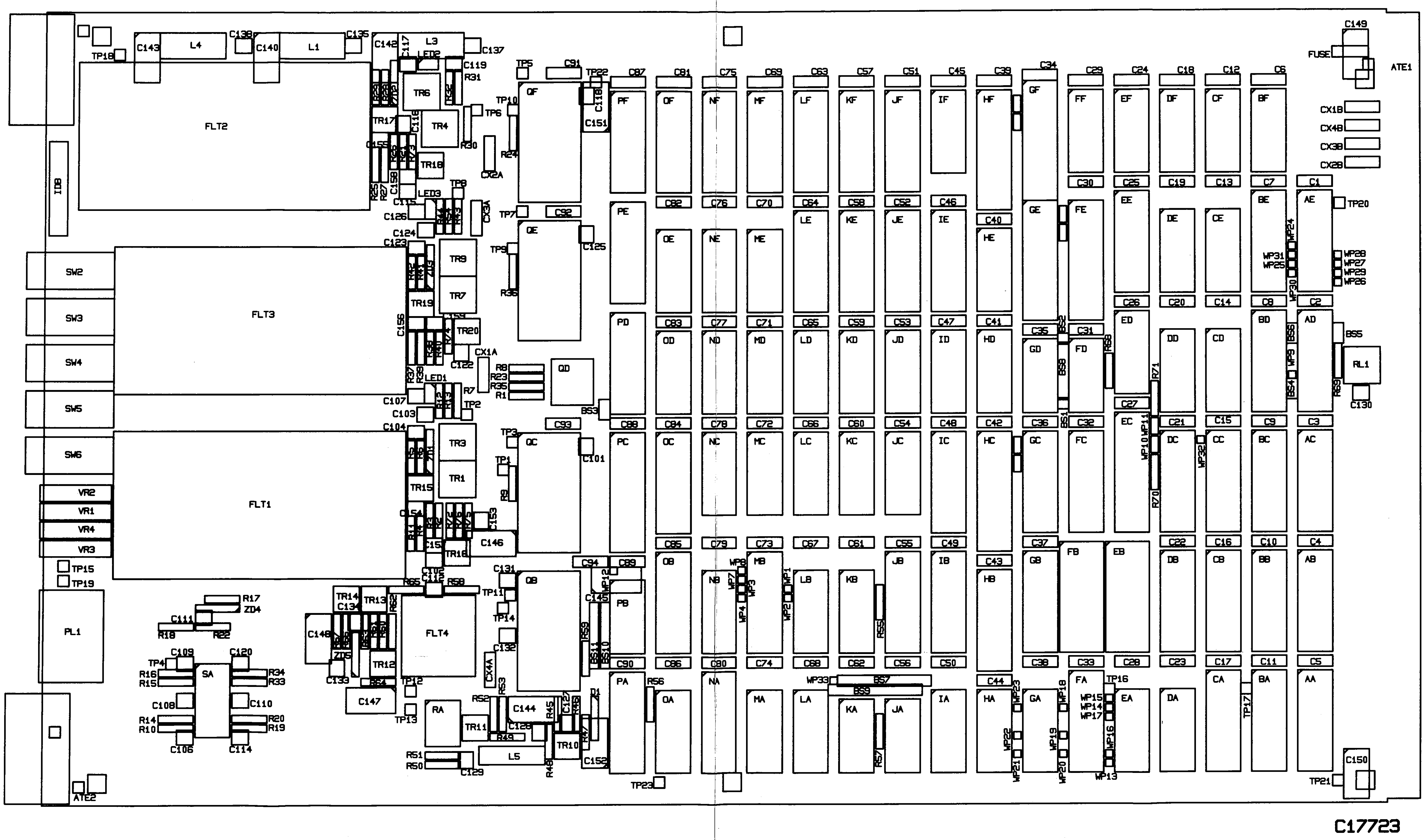


FIGURE 4.18.3 17723C RGB OUTPUT CIRCUIT 1

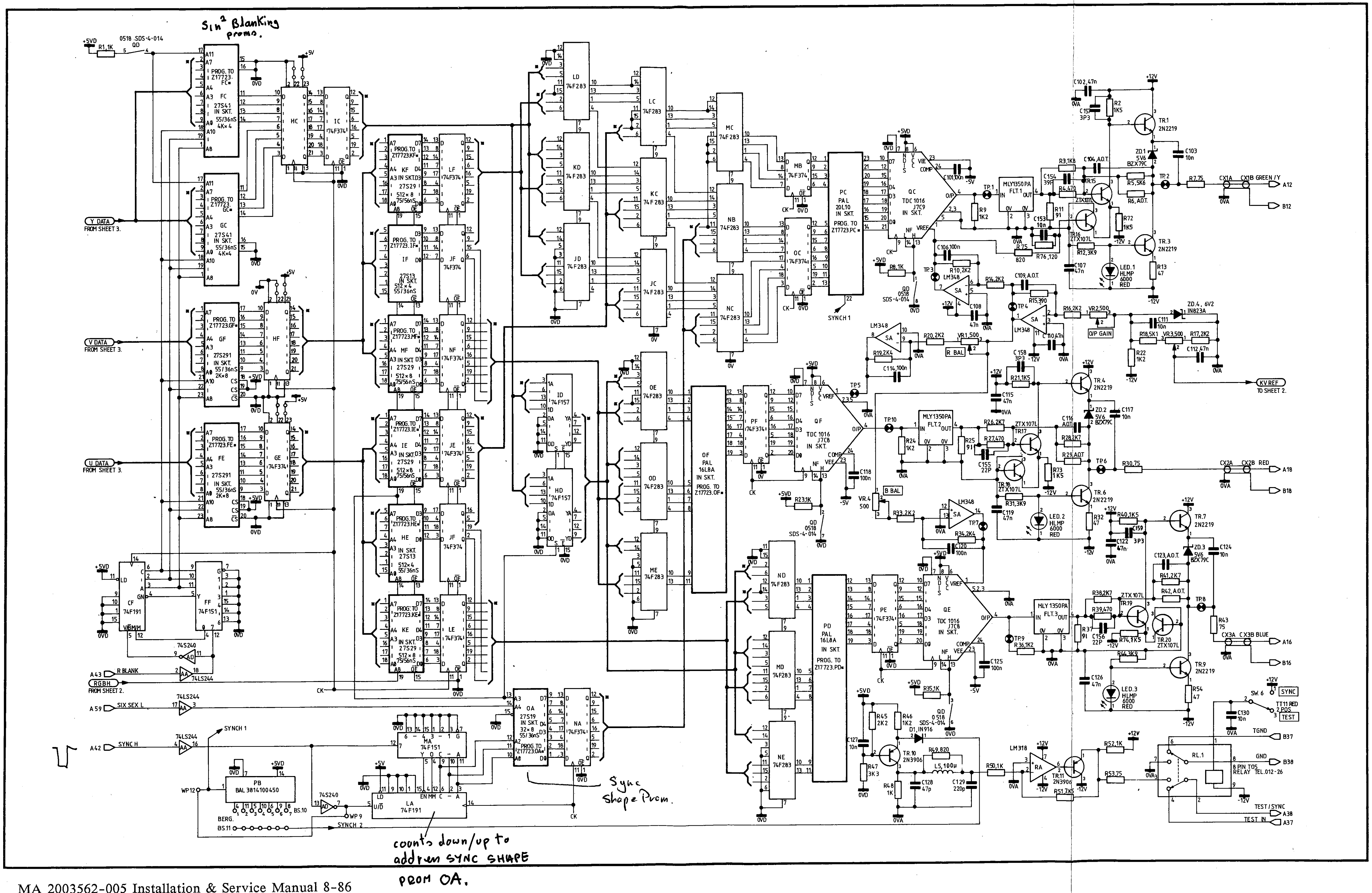


FIGURE 4.18.4 17723C RGB OUTPUT CIRCUIT 2

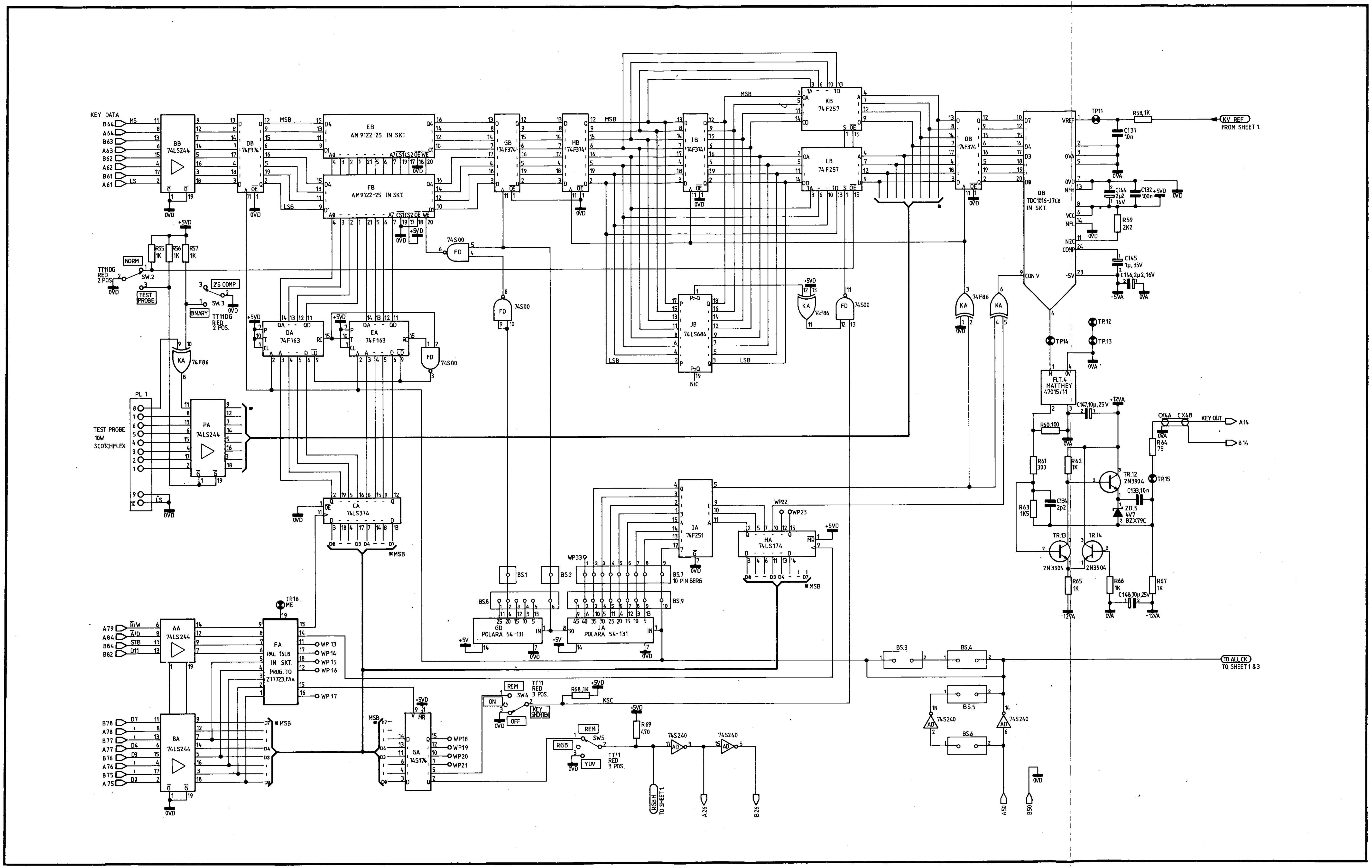
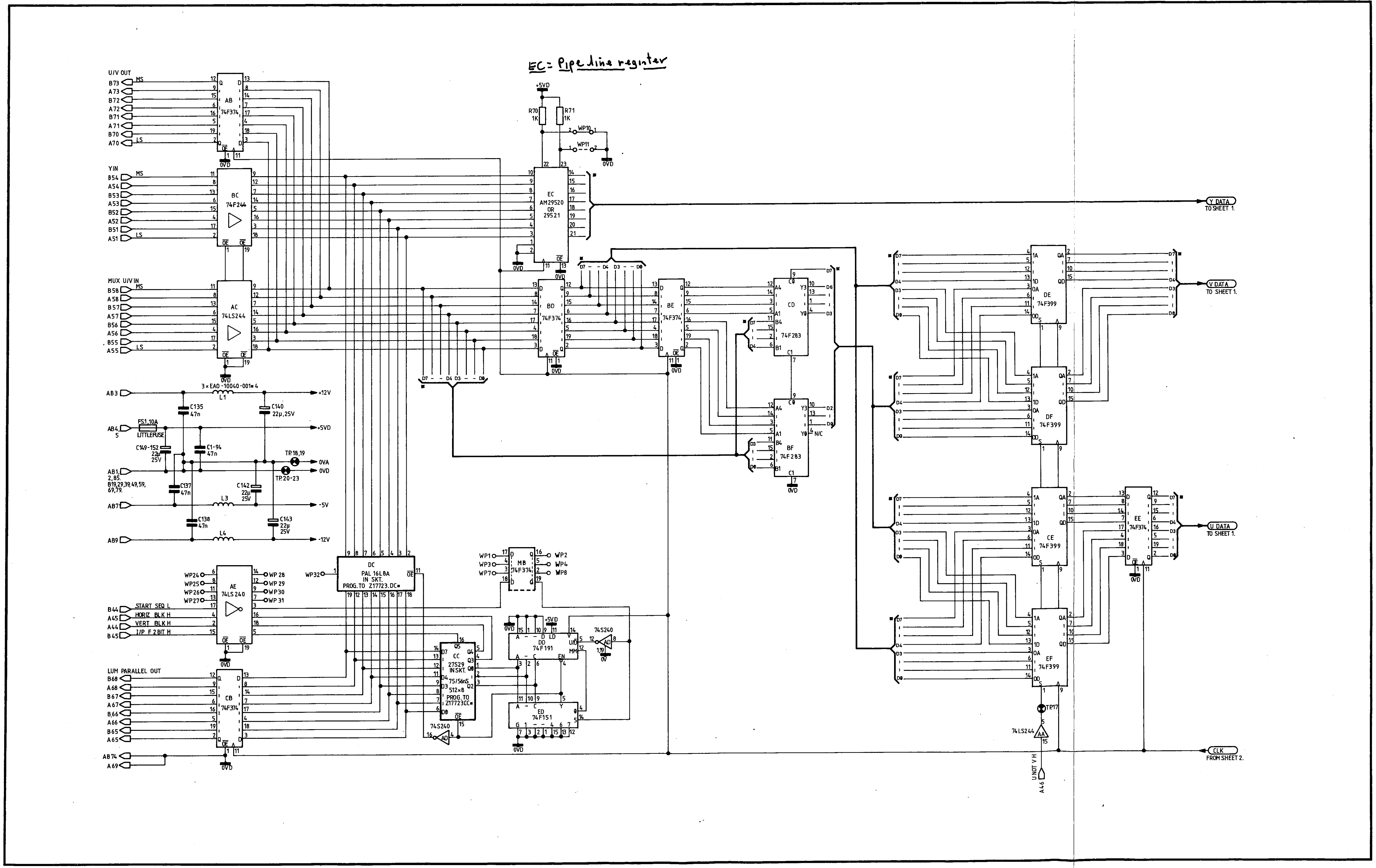


FIGURE 4.18.5 17723C RGB OUTPUT CIRCUIT 3


EC= Pipe line register

TIME CODE AND CUING CARD 17724C

(4,19C)

4:19:1 Function

The function of this card is to decode the Vertical Interval Time Code (VITC) and Longitudinal Time Code (LTC) to provide Match Frame editing facilities.

This card also provides output and input cue lines which enable the Harry system to cue external devices and to be cued from a number of different sources.

4:19:2 Circuit Description

(a) VERTICAL INTERVAL TIME CODE

The VITC (Input video) signal is buffered by BE (TP7), filtered and passed the comparator circuit DE and associated components. The filtered video signal is sampled during burst position by the sample and Hold circuit TR1, TR2, TR3 and DF, and the sampled voltage produced is passed to the comparator DE via the amplifier DF and VR1 (threshold level).

The TTL serial Time code data produced by the comparator DE (TP8) is clocked into the shift register HF, and the parallel data produced is clocked into the RAMs IC, ID or HC, HD. The system computer then reads the stored Time code data via the selected buffer GB or HB. The selector circuit IE and HE selects write addresses and enables for one pair of RAMs while read addresses and enables are selected for the other pair.

The Time code data from DE triggers the latch MF during the valid data window. This is produced by the monostable ME and KF. When MF is triggered, the counter FE is cleared and the bit rate clock is locked to the Time code data. The counter LE is clocked by the bit rate clock and produces a pulse at the end of each byte. This pulse is passed to the counter FE, via the latch LF and the monostable IF, to synchronize the bit rate clocks and the serial Time code data.

The byte clock produced by LE is used by the data shift register HF to load the parallel data into the RAMs IC, ID or HC, HD. This clock is also used to clock the byte counter GF, to provide the write addresses for the RAMs IC, ID or HC, HD.

(b) CYCLIC REDUNDANCY CHECK

The CRC byte on the Time code is checked against the calculated CRC from the Time code data. This is done by the CRC checking circuit MD, KE and JE. This circuit checks each bit of the Time code data as it is received. The final calculated CRC is then compared with the transmitted CRC, to produce zero in the shift register KE. This is detected by the comparator JE which produces the VITC received flag. This flag then is used to determine whether the Time code data in the RAMs is to be over-written.

(c) LONGITUDINAL TIME CODE

The LTC signal from the socket on the back panel is filtered and attenuated then amplified by the balanced amplifier circuit OD and associated components. The signal produced is then filtered by the active filter circuit OD and associated components, to provide the input signal for the comparator circuit OB and associated components.

The positive and negative edges of the LTC data clock the monostables OA to produce pulses on each data edge at MC pin 8. These pulses clock the latch KA and the monostable NB to produce data bits. The serial bit stream produced by KA is clocked into the shift registers KB and LA, which produce parallel data bytes and the sync words. The sync words from KB and LA are detected by LC, LB, KF and KA, which reloads the bit counter LD at the end of each byte.

The data bytes from KB are written into the RAMs JA, JB or IA, IB and read by the system computer via the selected buffer GA or HA. The selector circuit JC and JD selects write addresses and enables for one pair of RAMs while read addresses and enables are selected for the other pair.

The bit rate clocks produced by NB clock the counter LD, which counts the bits in each byte. The byte rate clocks produced by LD clock the byte counter KD to produce the write addresses for the RAMs JA, JB or IA, IB.

(d) INPUT AND OUTPUT CUE LINES

The 4 input cue lines from the Remote socket on the rear panel are passed to the input of the buffer CB, which is enabled onto the system computer bus by the decode PAL DB. The cue inputs are read by the system computer each video field just after the field group.

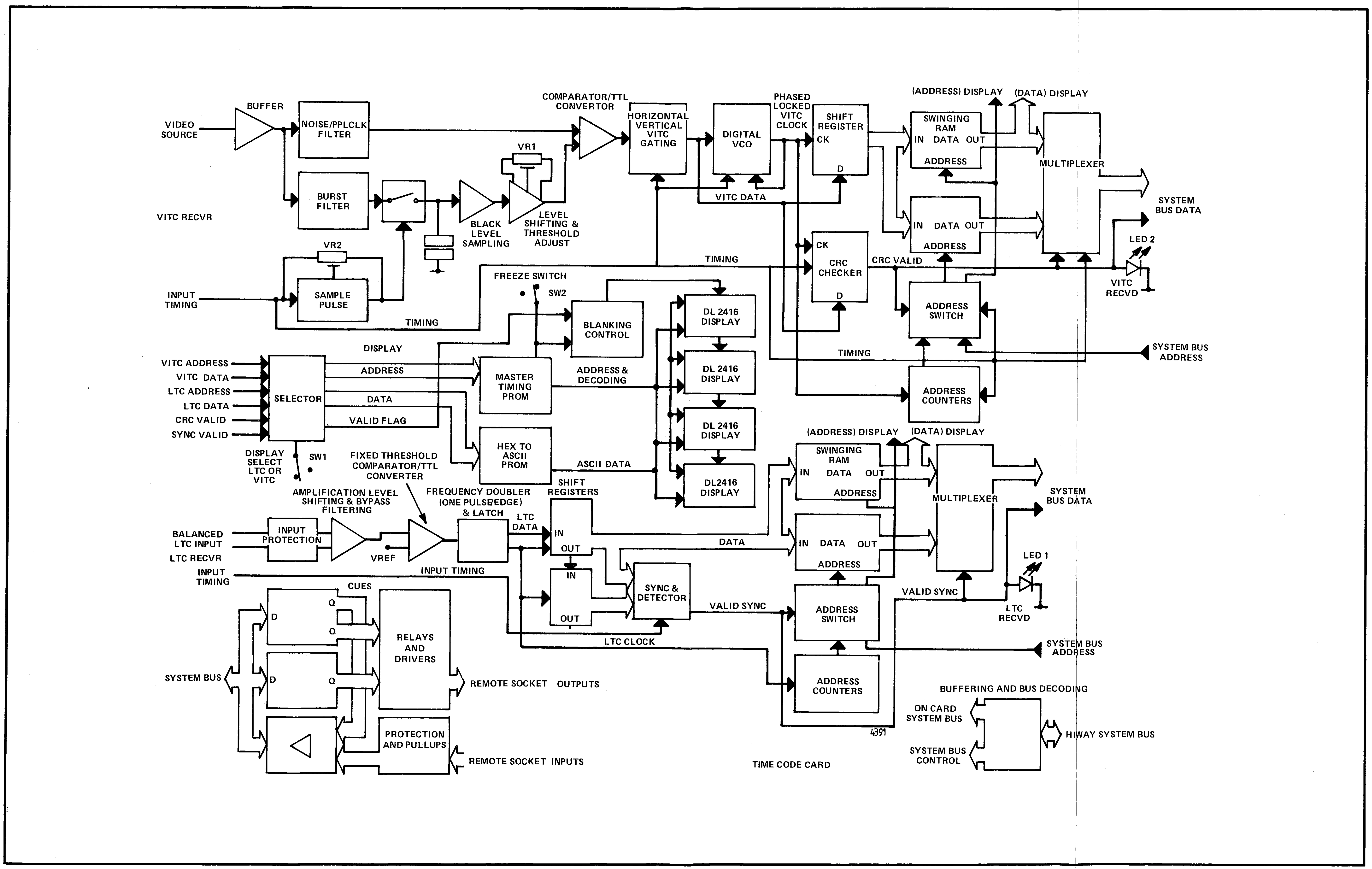
The data held in the computer loaded registers CA and FB determine which of the 12 output cues are activated. Each output from these registers turns on a transistor which activate the appropriate relay contact closure. The relay contact pairs are connected directly to the Remote socket on the rear panel.

(e) COMPUTER BUS DECODE

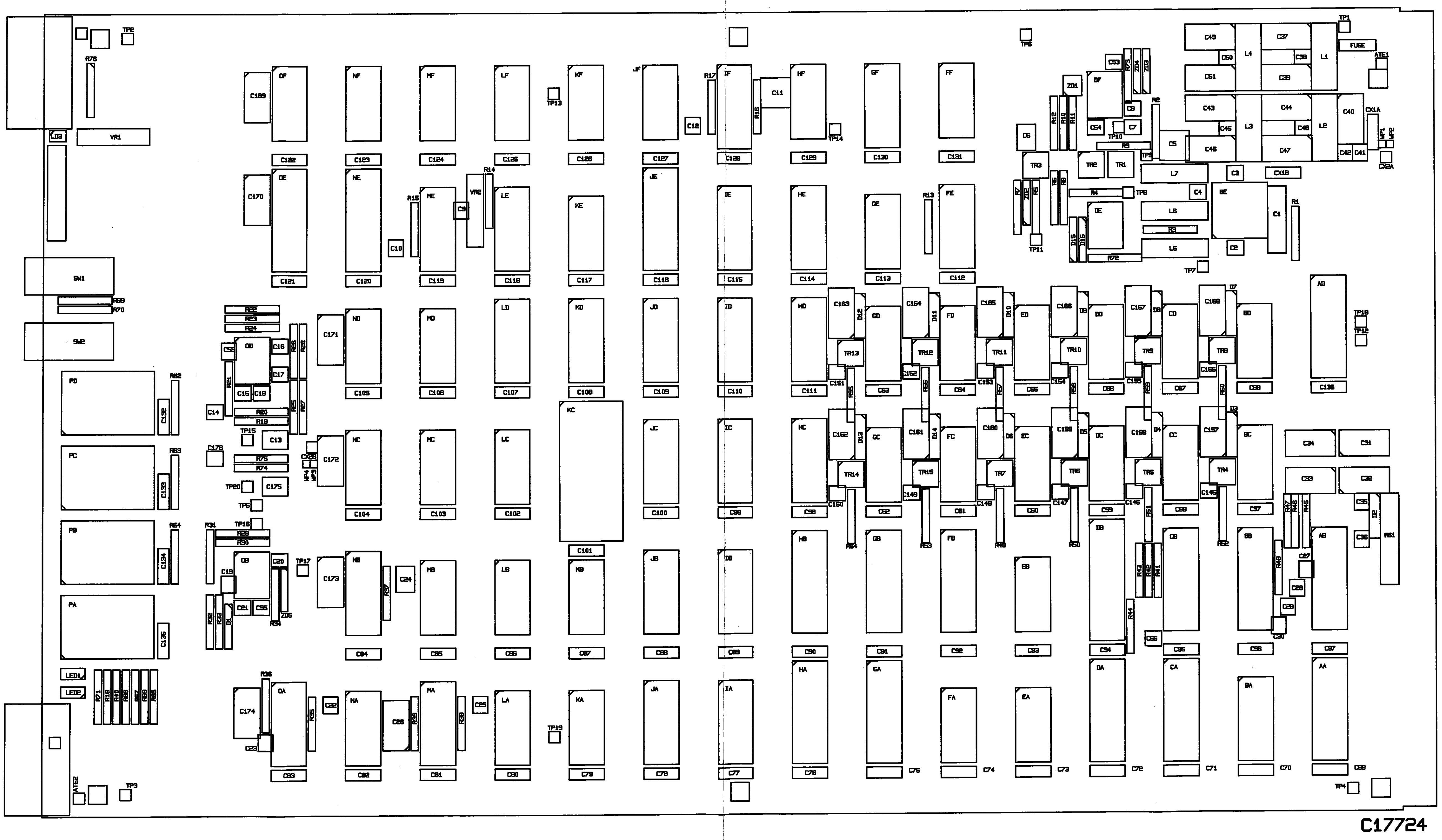
The system computer bus is buffered is CB, AB and AA and decoded by the Prom BA and the PAL DB to produce the clocks and enables for the computer controlled circuitry on this card.

(4,19C)

FIGURE 4.19.1 17724C TIME CODE BLOCK



(4,19C)
FIGURE 4.19.2 17724C TIME CODE LAYOUT



(4,19C)

FIGURE 4.19.3 17724C TIME CODE CIRCUIT 1

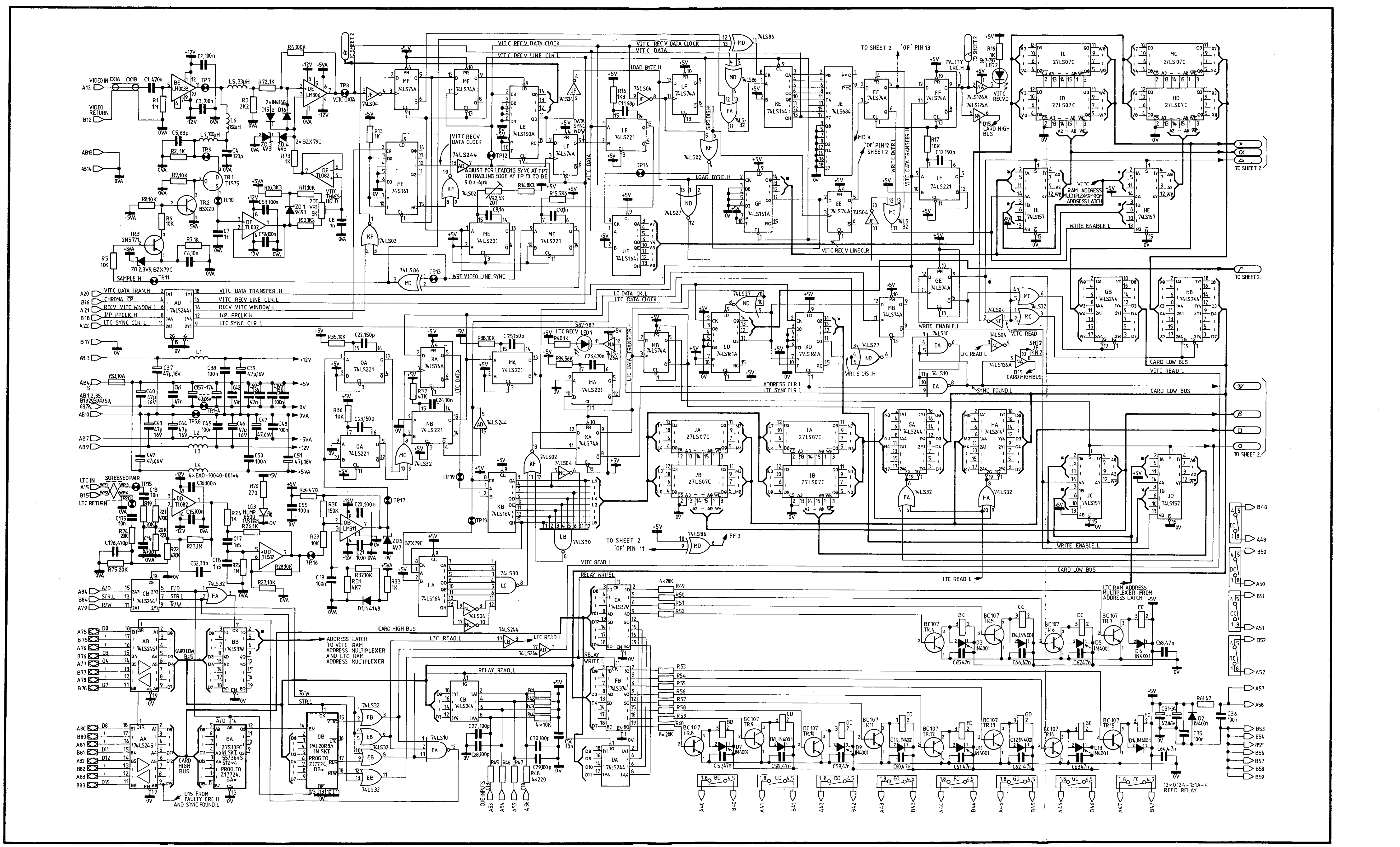
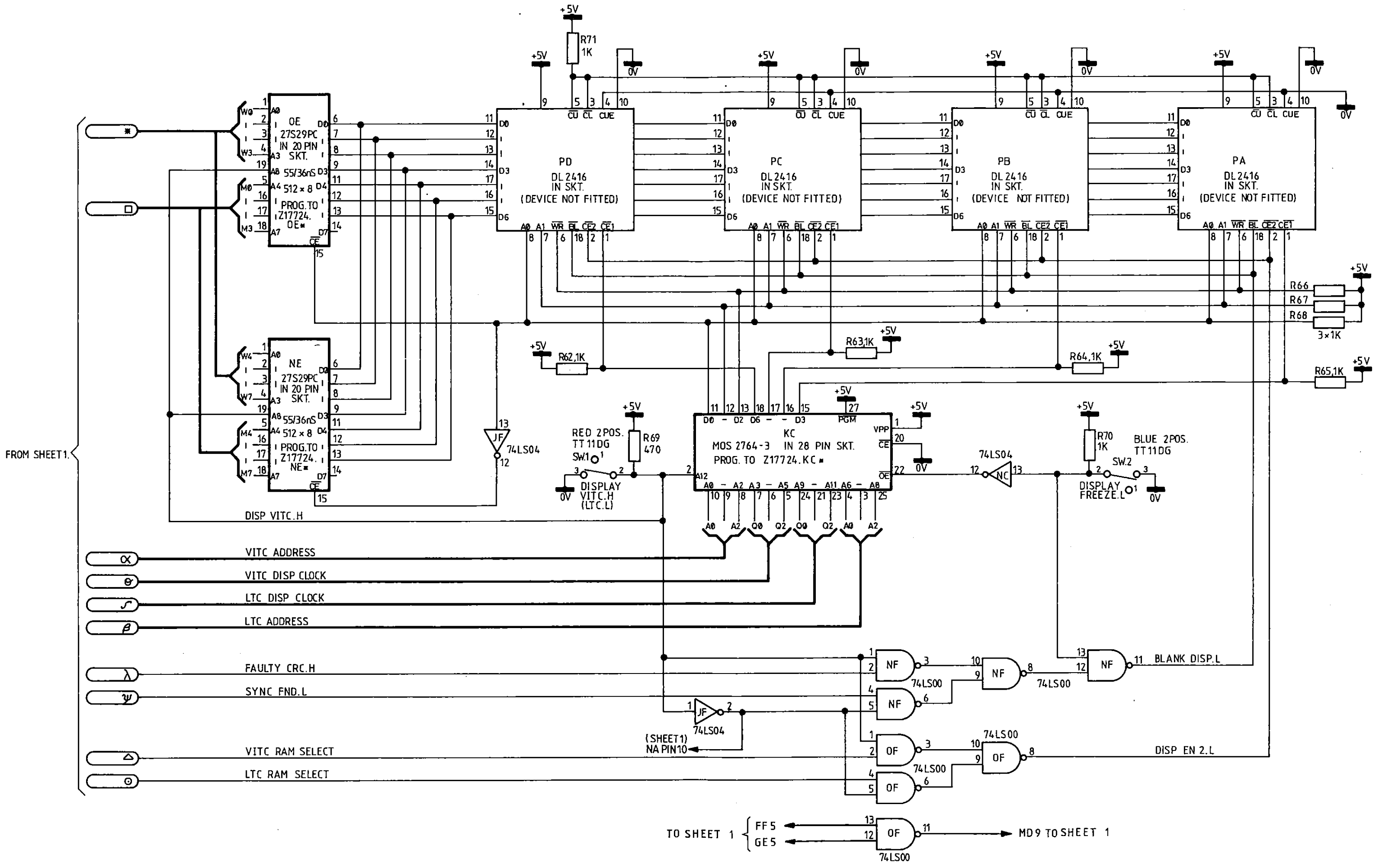


FIGURE 4.19.4 17724C TIME CODE CIRCUIT 2



IC. POWER CONNECTIONS.

TYPE	-12V	+12V	0V	TYPE	0V	+5V
LH0033	9,10	1,12		14 PIN DIL	7	14
LM 306	4	8	1	16 PIN DIL	8	16
TL 082	4	8		20 PIN DIL	10	20
LM 311	4	8	1	24 PIN DIL	12	24
				28 PIN DIL	14	28

RGB INPUT CARD 17727C

4:20:1 Function

The function of this card is to buffer, black level clamp, convert the Red, Green and Blue input signals into digital, and then Matrix them to produce Y and U/V data for the system. This card is an option which also can be configured for Y.U.V. input signals.

4:20:2 Circuit Description

(a) GREEN PATH

The Green input signal is AC coupled and buffered by the amplifier circuit TR1, the OP Amp SF and TR2. The Green signal is clamped on the Gate of TR3 by the sampled error voltage from SE. The clamped Green signal from TR3 is passed to the amplifier circuit RE, TR8, TR9, TR10, TR11 and TR12, whose output is filtered by FL1. The Filtered Green signal is buffered by TR24 into the ADC PF.

The Green data from PF is clocked through the register OF into the comparator OE, where the Green data is compared with the clamp value held in the computer loaded register GB. The output from OE is sampled by NA to provide the Black level sample for the Sample and Hold circuit SE and associated components.

The Green data from OF is passed to the input of the register MF, where the Test Green video data from the Prom NF can be selected. The output from the register MF is passed to the Green scaling Proms KF and LF. The scaled data is clocked through the registers IF and LE into the "Y" matrix.

(b) RED PATH

The Red input signal is AC coupled and buffered by the amplifier circuit TR4, and the OP Amp SD. The Red signal is clamped on the Gate of TR5 by the sampled error voltage from SD. The clamped Red signal from TR5 is passed to the amplifier circuit RC, TR13, TR14, TR15, TR16 and TR17, whose output is filtered by FL2. The Filtered Green signal is buffered by TR26 into the ADC PD.

The Red data from PD is clocked through the register OD into the comparator ND, where the Red data is compared with the clamp value held in the computer loaded register FA. The output from ND is sampled by NA to provide the Black level sample for the Sample and Hold circuit SD and associated components.

The Red data from OD is passed to the input of the register ME, where the Test Red video data from the Prom NE can be selected. The output from the register ME is passed to the Red scaling Proms JF and JE. The scaled data is clocked through the registers HF and LE into the "Y" matrix.

(c) BLUE PATH

The Blue input signal is AC coupled and buffered by the amplifier circuit TR6, and the OP Amp SB. The Blue signal is clamped on the Gate of TR7 by the sampled error voltage from SA. The clamped Blue signal from TR7 is passed to the amplifier circuit RA, TR18, TR19, TR20, TR21 and TR22, whose output is filtered by FL3. The Filtered Blue signal is buffered by TR28 into the ADC PB.

The Blue data from PB is clocked through the register OB into the comparator OC, where the Blue data is compared with the clamp value held in the computer loaded register FB. The output from OC is sampled by NA to provide the Black level sample for the Sample and Hold circuit SA and associated components.

The Blue data from OB is passed to the input of the register MD, where the Test Green video data from the Prom NC can be selected. The output from the register MD is passed to the Blue scaling Proms JD and MC. The scaled data is clocked through the registers ID and JC into the "Y" matrix.

(d) Y MATRIX

Scaled Green data from IF and LE is passed to the adder circuit EF, GF and LC, where scaled Red data from HF and LE is added. The Green plus Red data produced is passed to the adder circuit DF, FF and KC, where the scaled Blue data from ID and JC is added. The Y data produced is clocked through the registers CE and JC into the invertor circuit EE, DE and IC, and into the pipe line register AE. The output from this register is buffered by AD and passed to the RGB Processor card.

(e) V MATRIX

Inverted Y data from EE, DE and IC is passed to the adder HE, GE and HC, where Red data from IE is added. The V data produced is clocked through the registers FE and FC, and scaled by the Prom ED. The scaled V data is clocked through the register CD, buffered BD then passed via the RGB Processor card to the Chroma Filter card.

(f) U MATRIX

Inverted Y data from EE, DE and IC is passed to the adder HD, GD and GC, where Blue data from KD is added. The U data produced is clocked through the registers FD and FC, and scaled by the Prom EC. The scaled U data is clocked through the register CC, buffered BC then passed via the RGB Processor card to the Chroma Filter card.

(g) KEY PATH (Not Used)

The input Key video is buffered and black level clamped by the amplifier circuit TR29, TR30 and TR31. The clamped Key signal is amplified by the amplifier circuit TR32, TR33, TR34, TR35 and TR36, then passed through the discrete low pass filter into the comparator QA. The Key signal is compared with the computer generated voltage from the DAC PA, to produce a TTL Key on the output of QA.

The digital Key is passed through the three-state buffer KA (which selects between digital or analogue sliced KEY) into the fine Key delay circuit KB and JB, controlled by DB. The output from the fine delay circuit is passed to the coarse delay circuit IB, HB, IA, HA and EB, controlled by the computer loaded register DB. The delayed Key signal is then passed to the Vertical Filter card.

(h) COMPUTER BUS DECODE

The system computer bus is buffered by BA and CA, and decoded by the PAL EA, to provide the enables for the computer controlled circuitry on this card.

4:20:3 Diagnostics

(a) SW1 VIDEO/TEST

This switch when in the down position enables the test video selected by Switch 2

(b) SW2 TEST VIDEO

This rotary switch selects various monochrome ramps which can be passed down the Red, Green and Blue paths in various combinations.

(c) SW 3 RAMP/MULTIBURST

This switch selects between digitally generated Ramp and digitally generated Multiburst test videos.

(d) SW5 RGB/YUV

This switch in conjunction with links on this card determines whether the card accepts RGB or YUV input video signals.

(e) VR3

This is the preset adjustment for GREEN or Y Gain.

(f) VR1

This is the preset adjustment for RED/BLUE Gain or U/V Gain.

(g) VR2

This is the preset adjustment for RED/BLUE balance or U/V balance.

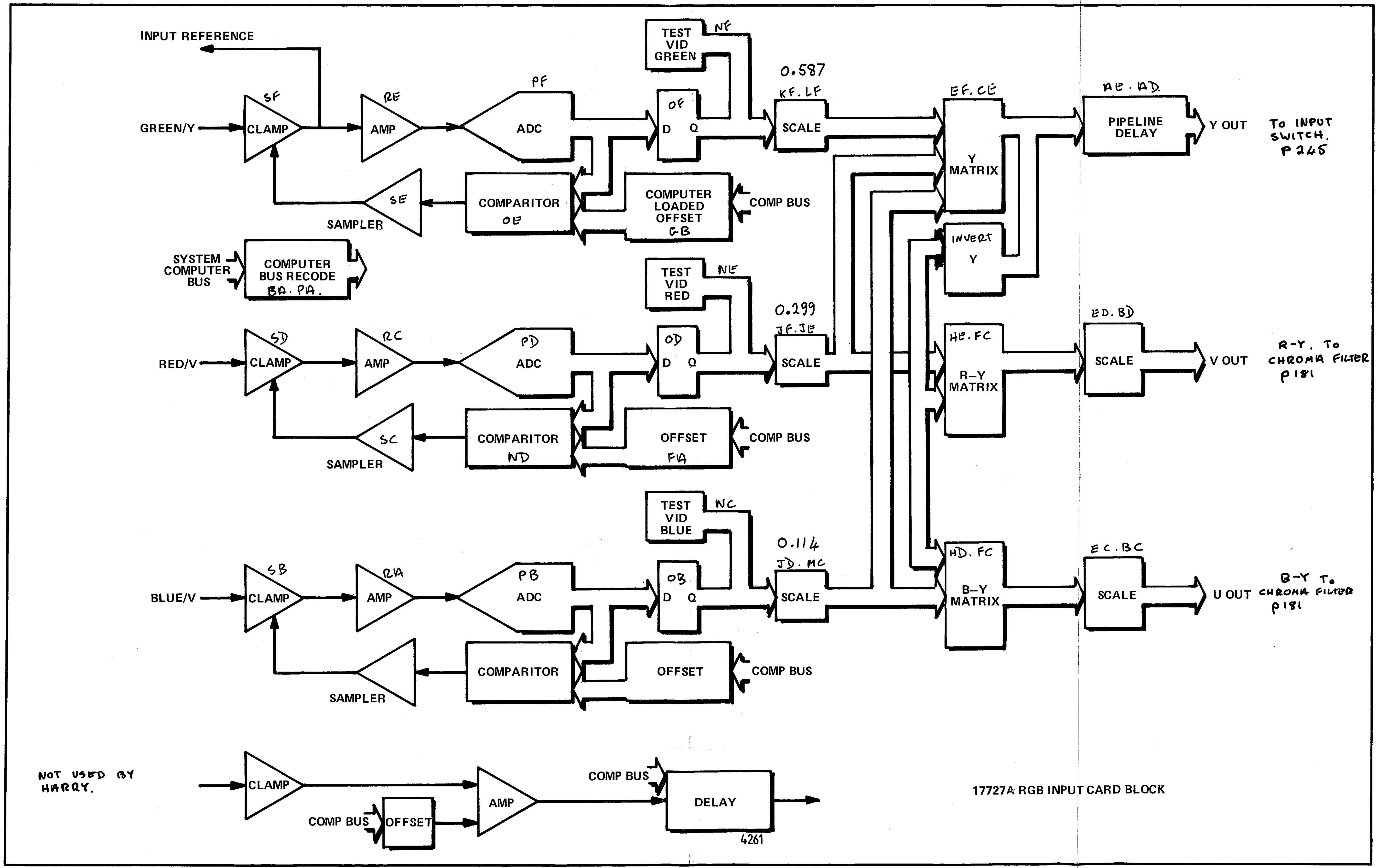
(h) VR4 (Not Used)

This is the preset adjustment for Input KEY Gain.

Caution: All links are factory preset. Do not adjust unless advised.

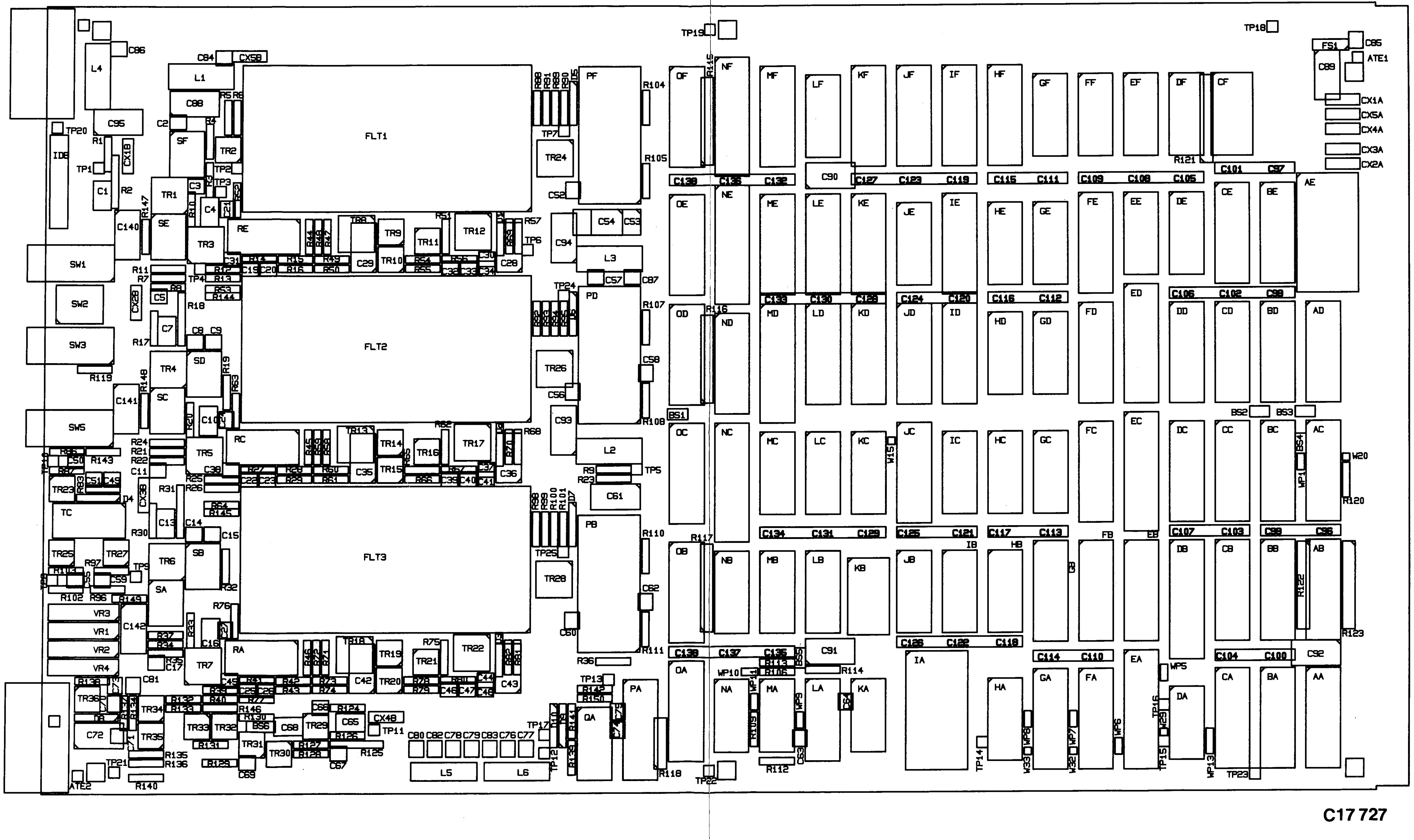
(4,20C)

FIGURE 4.20.1 17727C RGB INPUT BLOCK



(4,20C)

FIGURE 4.20.2 17727C RGB INPUT LAYOUT



To "input reference" in the event of Syncs on GREEN

VR3 GREEN GAIN (RGB) [Y gain YUV]

QUANTEL

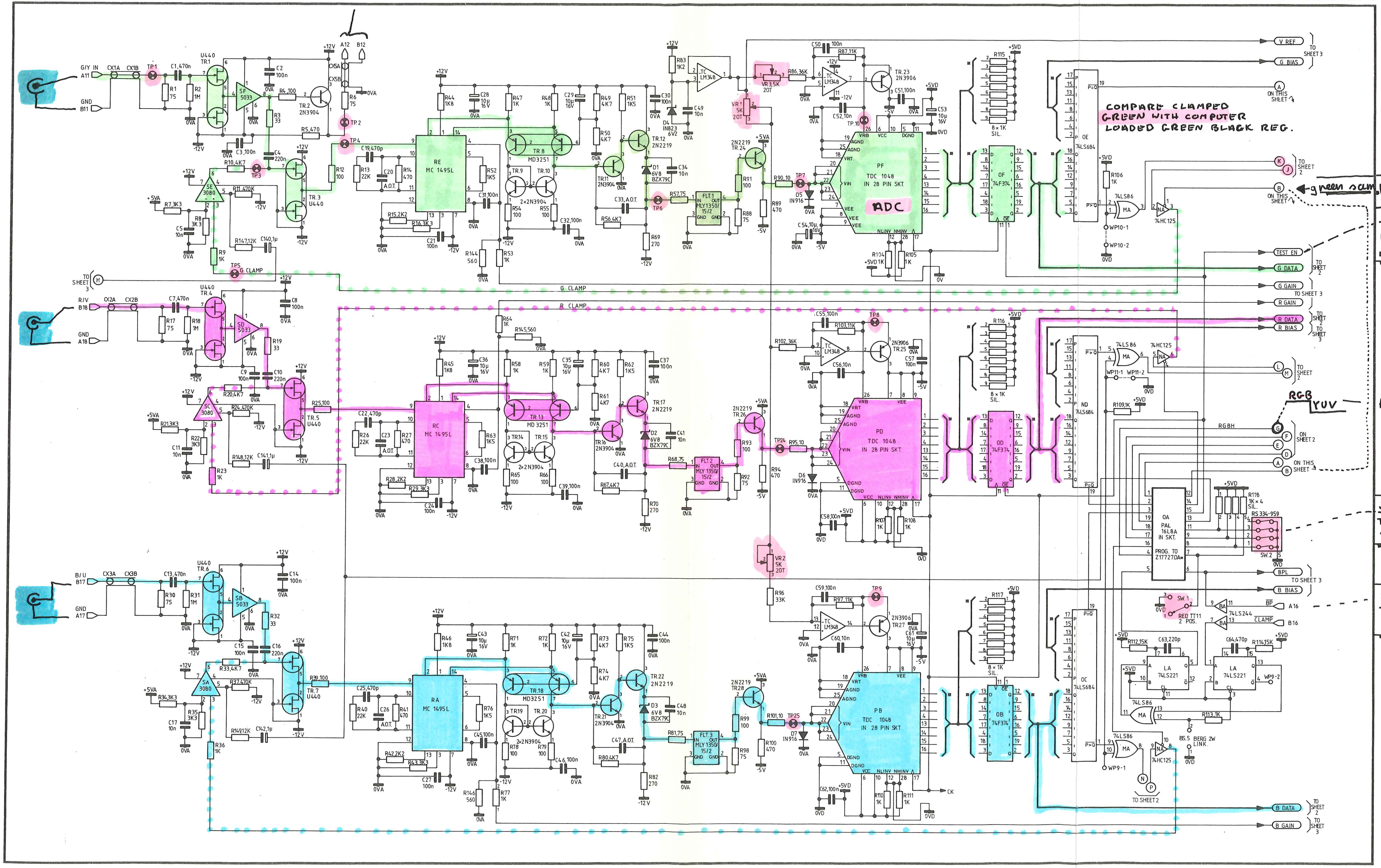
VR1 REDGAIN [inc BLUE] RGB (U/V Gain YUV)

VR2 BLUE GAIN [do red 1.st!] RGB (U/V Bal YUV)

(4,20C)

FIGURE 4.20.3 17727C RGB INPUT CIRCUIT 1

BE23



from sh3

H: disable R,G,B Latches in Test.

SW2 RAMPS TEST SIG SELECT.

SW1 TEST SIG ENABLE

(4,20C)

FIGURE 4.20.4 17727C RGB INPUT CIRCUIT 2

BE23

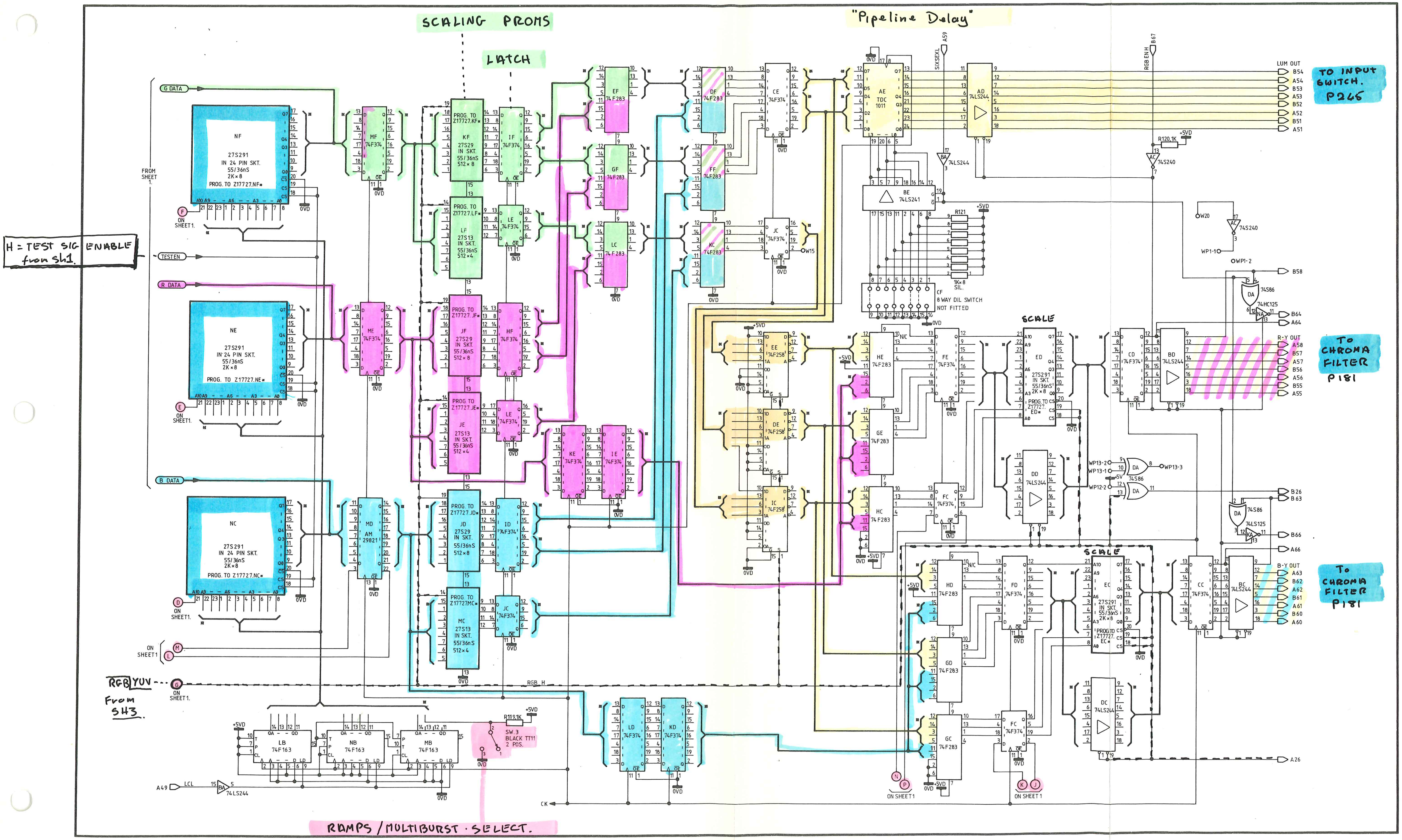
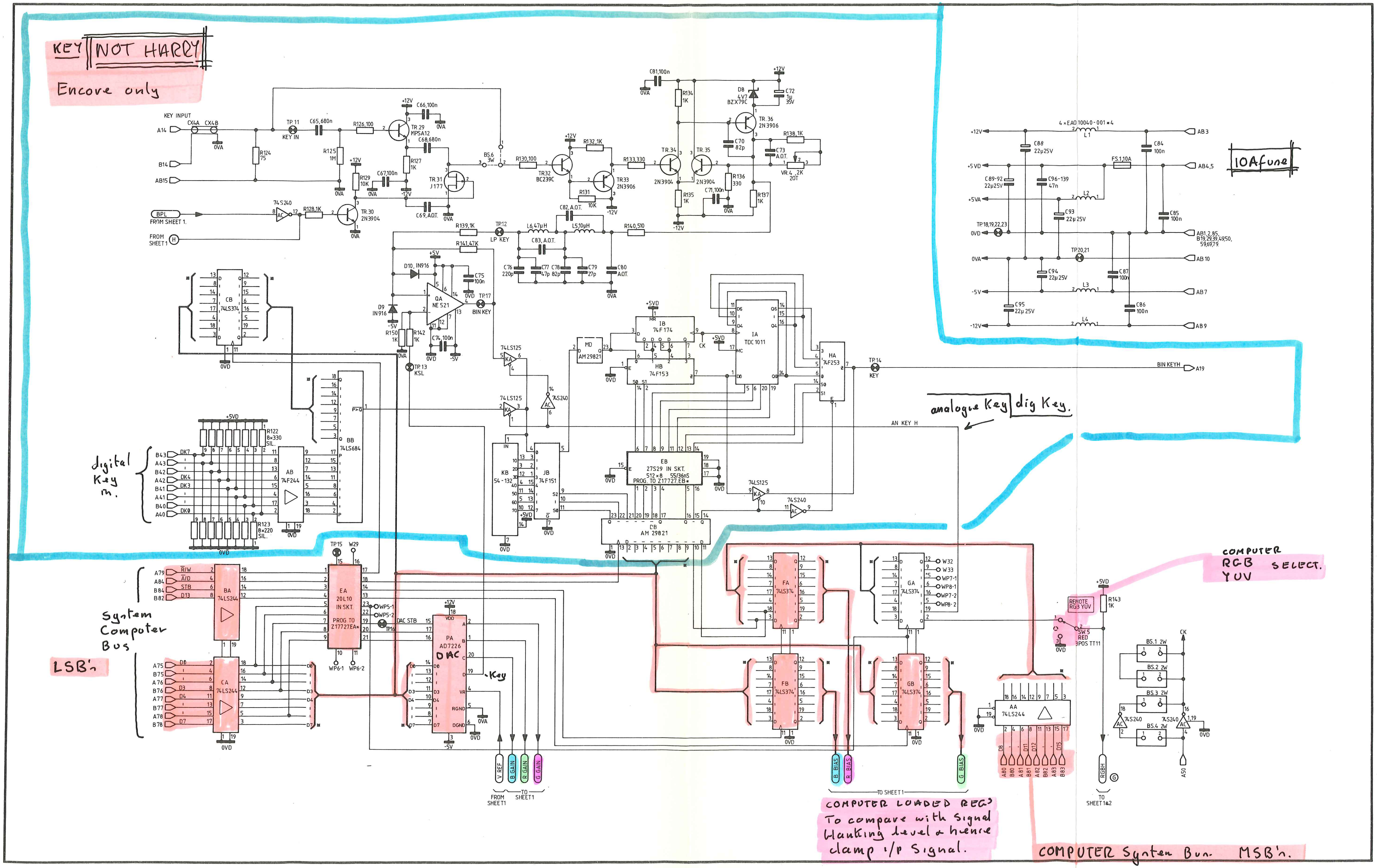


FIGURE 4.20.5 17727C RGB INPUT CIRCUIT 3

BE23



ROM/RAM CARD 17728A

4:21:1 Function

The function of this card is to store the system operating software and to provide non-volatile RAM for storing system constants such as Engineering setups and Disc Directories.

This card can be configured to provide addressed areas of Eprom and Non volatile Static RAM. The card consist of the three blocks which are linked for Eprom or RAM use. Each Block is addressed from the system computer and accessed via the 68000 bus from the CPU card.

4:21:2 Circuit Description

(a) ADDRESS DECODING

Addresses from the CPU card are buffered by AJ, AI and AH, and decoded by the PAL BH to provide enable signals for the data paths and the chip select decoders. The PALs BG, BE and BD provide individual enables for the Eproms or RAMs within each of the three Blocks. The Blocks are designated for Eprom or Static RAM use by the links in the headers FI and GJ.

Each Eprom or RAM in each Block is addressed by the CPU card via the buffers BJ, BI, CJ and CI and the resistor packs DJ, EI, FJ, GI, HJ and II.

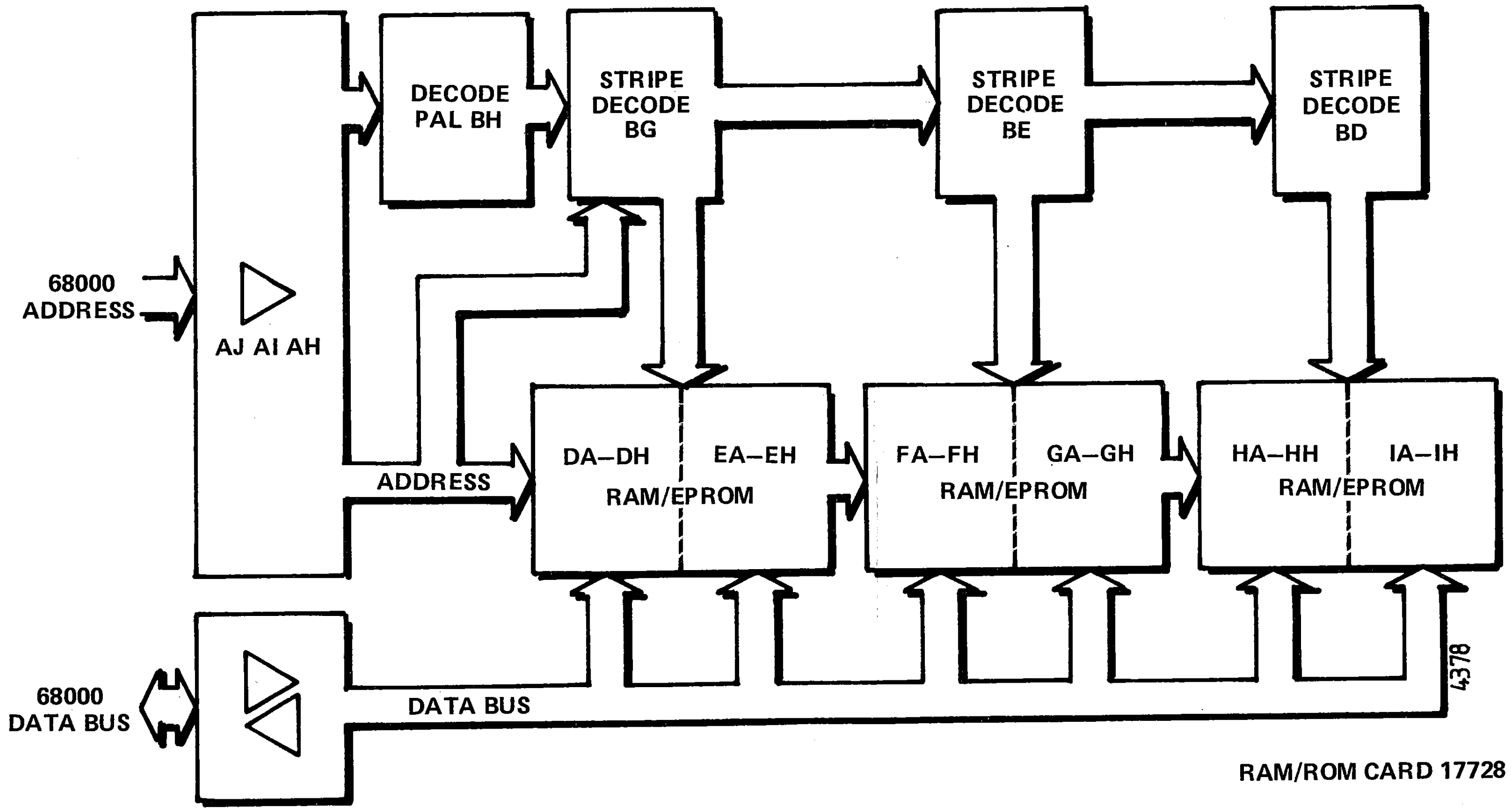
(b) DATA PATHS

The 68000 data bus from the CPU card is buffered by the bi-directional buffers AG, AE, AD and AC and connects with the Eproms and RAMs in each block. The direction of the data bus is controlled by the CPU card via BC and CD.

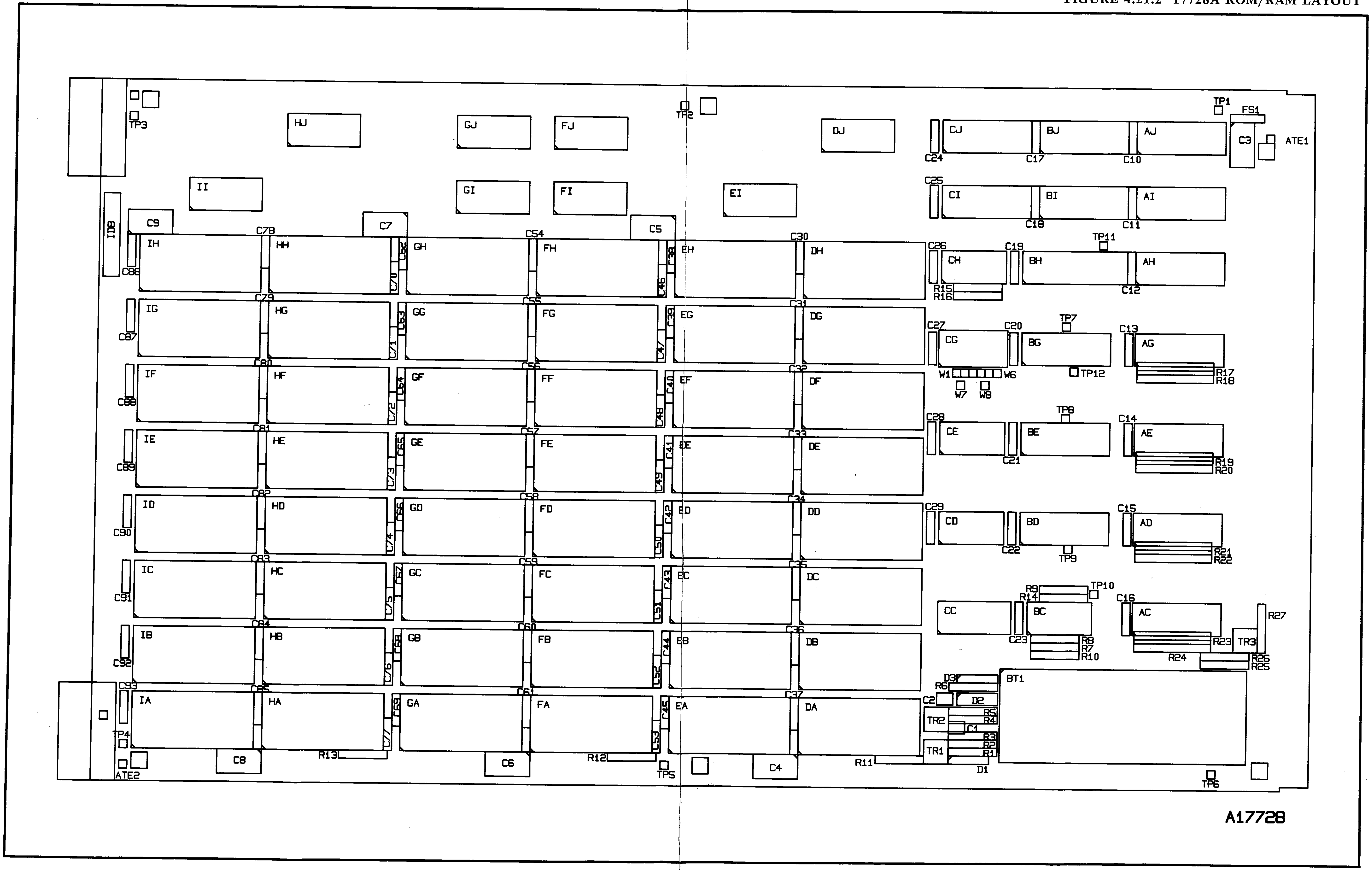
(c) BATTERY BACKUP SUPPLY

The battery BT 1 is continuously charged, when the system is on, via the constant current circuit consisting of TR1, TR2, TR3 and associated components. When the system +5 volt rail is missing the battery supplies the Static RAMs in the selected blocks. The 5 volt supply provided by the battery is passed to the Static RAMs via the selector links in the header CC.

(4,21A)
FIGURE 4.21.1 17728A ROM/RAM BLOCK

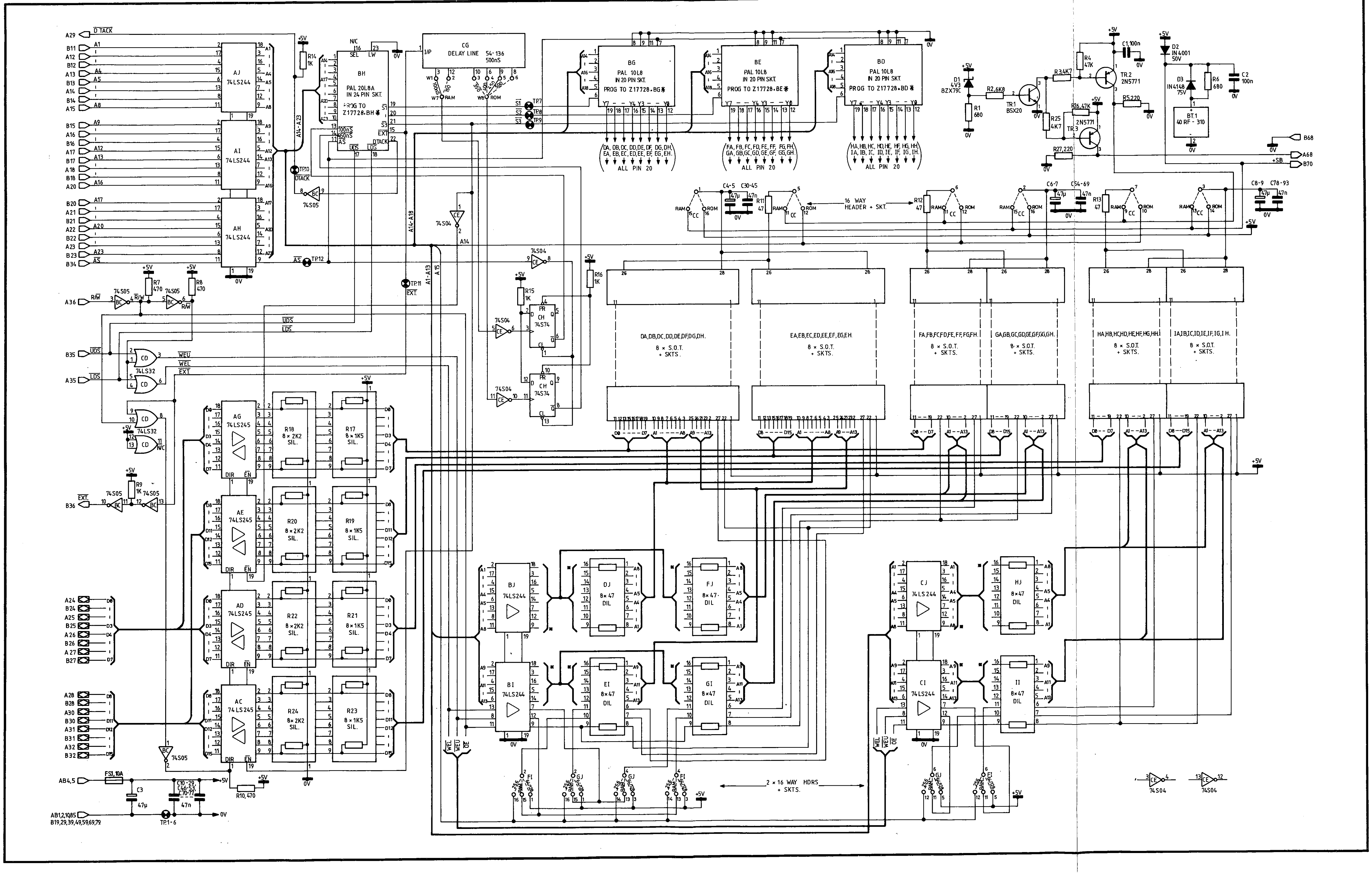


(4,21A)
FIGURE 4.21.2 17728A ROM/RAM LAYOUT



(4,21A)

FIGURE 4.21.3 17728A ROM/RAM CIRCUIT


AJ 74LS244
AI 74LS244
AH 74LS244
BH PAL 20L8A IN 24 PIN SKT. PROG TO Z17728-BH *
CG DELAY LINE 54-136 500nS
BG PAL 10L8 IN 20 PIN SKT. PROG TO Z17728-BG *
BE PAL 10L8 IN 20 PIN SKT. PROG TO Z17728-BE *
BD PAL 10L8 IN 20 PIN SKT. PROG TO Z17728-BD *
DA, DB, DC, DD, DE, DF, DG, DH, EA, EB, EC, ED, EE, EF, EG, EH. ALL PIN 20
FA, FB, FC, FD, FE, FF, FG, FH, GA, GB, GC, GD, GE, GF, GG, GH. ALL PIN 20
HA, HB, HC, HD, HE, HF, HG, HH, IA, IB, IC, ID, IE, IF, IG, IH. ALL PIN 20
D1 4V3 BZX79C
TR1 BSX20
TR2 2N5771
TR3 2N5771
D2 IN4001 50V
D3 IN4148 75V
BT1 40 RF-310
16 WAY HEADER + SKT.
DA,DB,DC,DD,DE,DF,DG,DH. 8 × S.O.T. + SKTS.
EA,EB,EC,ED,EE,EF,EG,EH. 8 × S.O.T. + SKTS.
FA,FB,FC,FD,FE,FF,FG,FH. 8 × S.O.T. + SKTS.
GA,GB,GC,GD,GE,GF,GG,GH. 8 × S.O.T. + SKTS.
HA,HB,HC,HD,HE,HF,HG,HH. 8 × S.O.T. + SKTS.
IA,IB,IC,ID,IE,IF,IG,IH. 8 × S.O.T. + SKTS.
CH 74S74
74S04
74S05
74LS32
AG 74LS245
AE 74LS245
AD 74LS245
AC 74LS245
R18 8 × 2K2 SIL.
R17 8 × 1K5 SIL.
R20 8 × 2K2 SIL.
R19 8 × 1K5 SIL.
R22 8 × 2K2 SIL.
R21 8 × 1K5 SIL.
R24 8 × 2K2 SIL.
R23 8 × 1K5 SIL.
BJ 74LS244
BI 74LS244
DJ 8 × 47 DIL
FJ 8 × 47 DIL
EI 8 × 47 DIL
GI 8 × 47 DIL
CJ 74LS244
CI 74LS244
HJ 8 × 47 DIL
II 8 × 47 DIL
2 × 16 WAY HDRS + SKTS.
FS1,10A
TP1-6
AB12,10&85 B19,29,39,49,59,69,79

DATA SELECT CARD 17730D

4:22:1 Function

There are 4 Data Select cards in the system; one in each satellite. The function of this card is to select data from the Mux Demux card, the Disc Interface card, the Combiner card and the Buffer Store, and pass the selected data to the Buffer Store, the I/O Store and Disc Interface card.

This card also holds circuitry used to generate Crop windows so that selected sections of the Buffer Store can be written.

4:22:2 Circuit Description

(a) DATA SELECTOR CIRCUIT

Satellite data from the Mux Demux card is clocked through the register AI and passed to the buffers BI, CI and DI. Disc data from the Disc Interface card is clocked through the register AE and passed to the buffers BE, CE and DE. Data from the Combiner card is clocked through the register AG and passed to the buffers BG, CG and DG. Switched Buffer Store data is clocked through the register AJ and passed to the buffers BJ, CJ and DJ.

The buffers BJ, BG, BE and BI are enabled by the Control register (A0 to A3) to form the Buffer Store data selector circuit. The output from the enabled buffer is clocked through the register AH and passed to the Buffer Store cards.

The buffers CJ, CG, CE and CI are enabled by the Control register (B0 to B3) to form the I/O Store data selector circuit. The output from the enabled buffer is clocked through the register AF and passed to the I/O Store.

The buffers DJ, DG, DE and DI are enabled by the Control register (C0 to C3) to form the Disc Interface data selector circuit. The output from the enabled buffer is clocked through the register AC and passed to the Disc Interface card.

(b) CLOCK SELECTOR CIRCUIT

Disc and Video clocks are buffered by AD and BC and passed to the buffers CB, DC and CC, which form the 2 clock selector circuits. The selected Disc or Video clock signals from CB and DC are buffered by AD and passed to the Crop circuit. The selected Disc or Video clock signals from DC and CC are buffered by AK and passed to the Buffer Store cards.

(c) CROP CIRCUIT

The FIFO circuit EH, ED and GF is loaded by the system computer with the horizontal Crop start and Crop length values. The horizontal counter circuit FG, FC and GC is clocked by picture point clocks (Disc or Video) and counts up from the loaded value held in the computer loaded FIFOs EG, EC and HA.

The horizontal counter counts up until the Crop start value is reached then the Magnitude comparator circuit FH, FD and GD gives equality. When this occurs HH produces the horizontal Write Enable signal, and the Crop length value is selected from the FIFO circuit EH, ED and GF. The horizontal counter continues to increment until the horizontal Crop length value is reached then the Write Enable signal is disabled.

The FIFO circuit EF, EB and HF is loaded by the system computer with the vertical Crop start and Crop length values. The vertical counter circuit FF, FA and GA is clocked by line clocks (Disc or Video) and counts up from the loaded value held in the computer loaded FIFOs EE and EA.

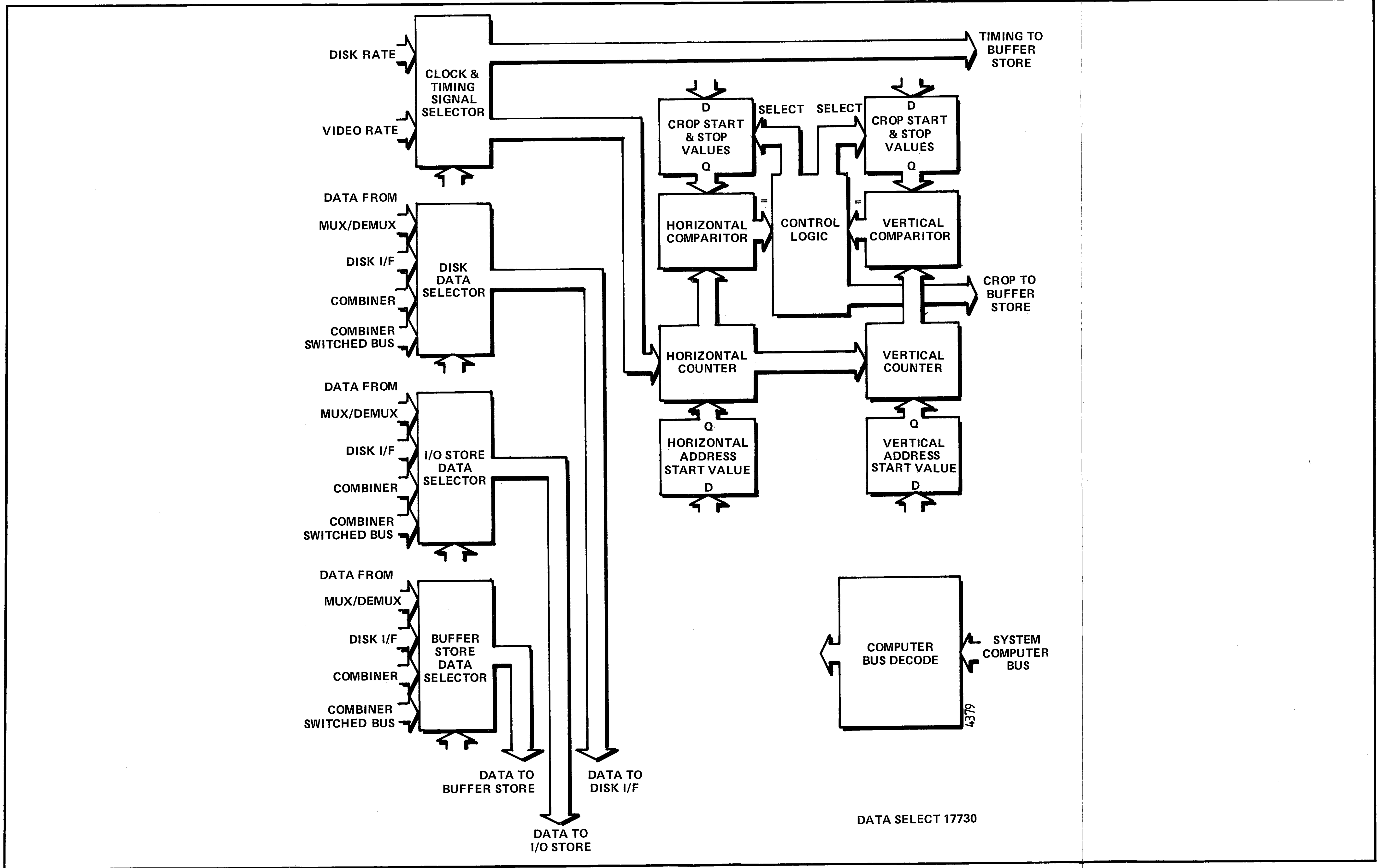
The vertical counter counts up until the Crop start value is reached then the Magnitude comparator circuit FF, FB and GB gives equality. When this occurs HE produces the vertical Write Enable signal, and the Crop length value is selected from the FIFO circuit EF, EB and HF. The vertical counter continues to increment until the vertical Crop length value is reached then the Write Enable signal is disabled.

The horizontal Crop is produced each video line and when both horizontal and vertical Crops occur the Write enable signal WEHN (A24) is passed to the Buffer Store cards to enable the writing process.

(d) COMPUTER BUS DECODE

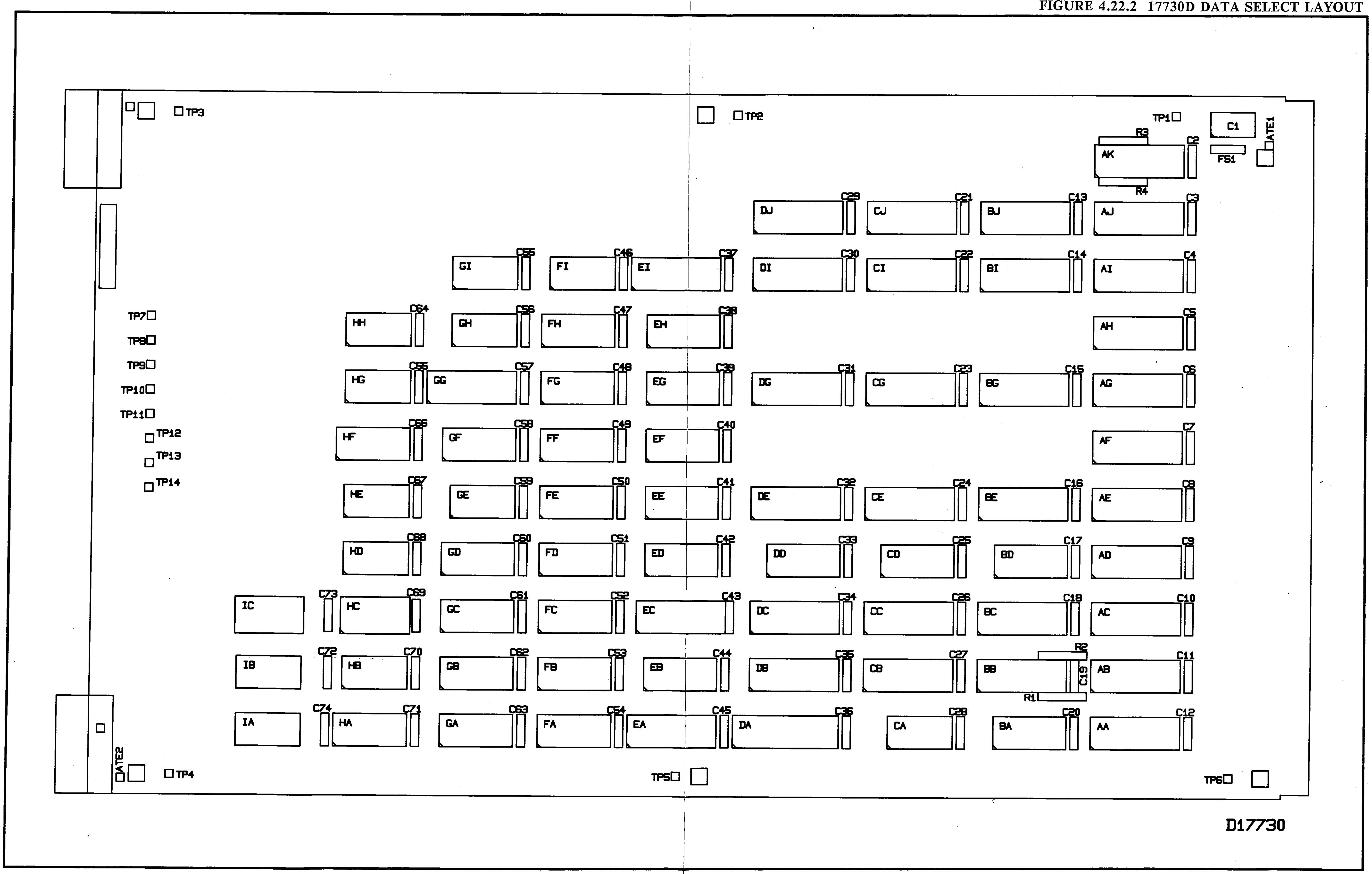
The system computer bus is buffered by BB, AA and AB, and decoded by the Prom BA and the PAL DA to provide the clocks and enables for the computer controlled circuitry on this card. The Control register GG and DB is loaded with the required selector functions, which are decoded by BD, DD and CD to provide the selector enable signals.

(4,22D)
FIGURE 4.22.1 17730D DATA SELECT BLOCK

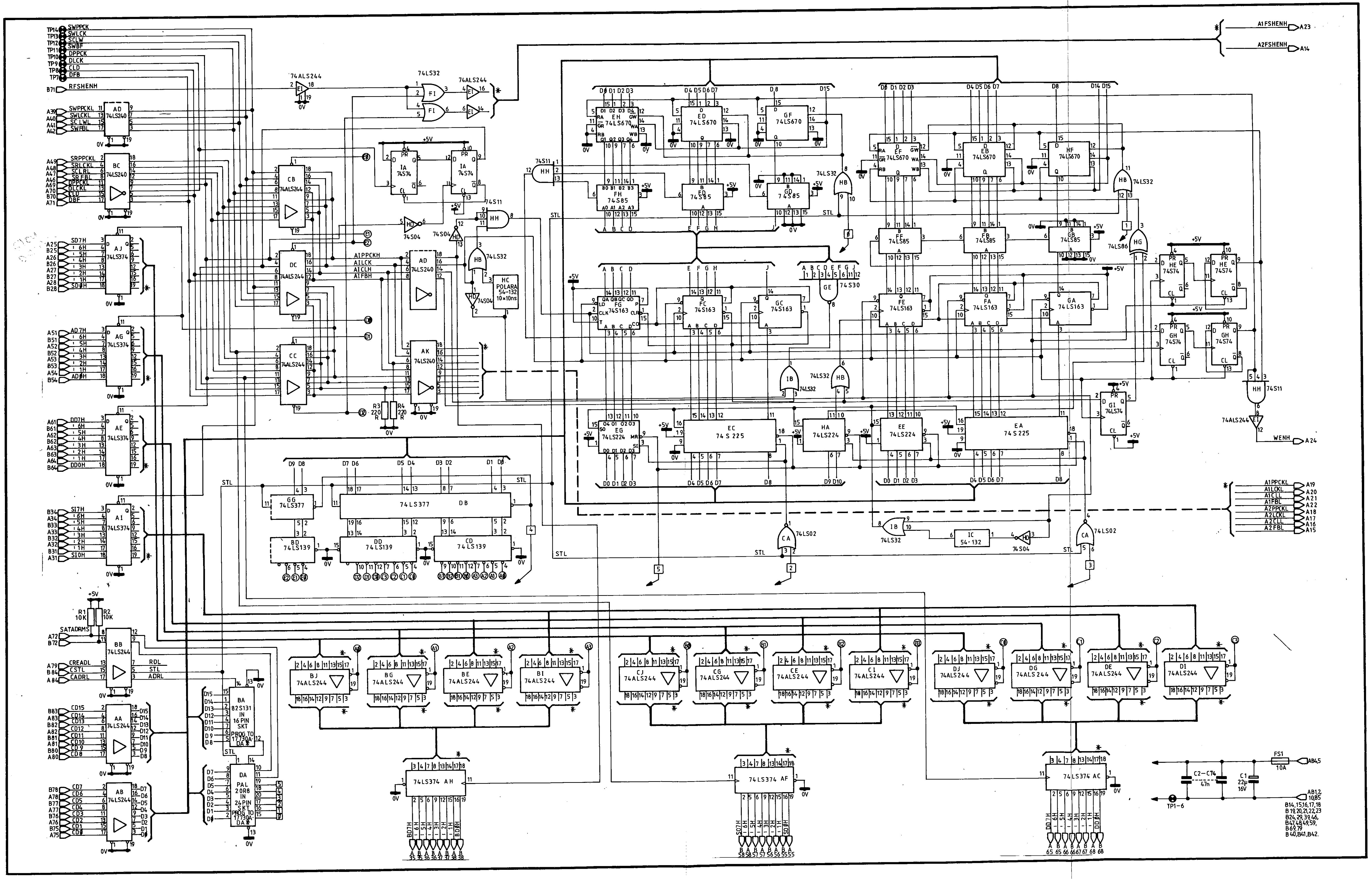


(4,22D)

FIGURE 4.22.2 17730D DATA SELECT LAYOUT



(4,22D)
FIGURE 4.22.3 17730D DATA SELECT CIRCUIT



COMBINER CARD 17732B

4:23:1 Function

There are 4 Combiner cards in the system, one in each satellite. The function of this card is to combine selected data from the system to produce dissolves, temporal filtering, Luminance keying, mixing and other effects. The Combiner has two channels A and B which are used to process two selected video sources and one channel C for keying from eight possible inputs sources.

4:23:2 Circuit Description

(a) CHANNEL SELECTOR CIRCUITS

Data from the system is selected by the three channel selector circuits as follows:

Input	**Channel A**	**Channel B**	**Channel C**
I/P 1A	AF	AE	AD
I/P 1B	BF	BE	BD
I/P 1C	CF	CE	CD
I/P 2A	DF	DE	DD
I/P 2B	EF	EE	ED
I/P 2C	FF	FE	FD
Bus	DG	FG	AC

The output data from the enabled register in each channel selector circuit is then passed to the data paths of channels A, B and C. The source selection is controlled by the system computer using the control register circuit CC, DC, EB, EC, FB and FC.

(b) CHANNEL A DATA PATH

Data from channel A's selector circuit is clocked through the register HF and passed to the Multiplier LF, where the data is scaled by the coefficient held in the computer loaded register OD. The scaled data produced is passed through the Exclusive ORs circuit IG, JD, JE and IF, where the 16-bit data can be inverted for channel subtraction. The register OF provides the data bypass path and PE sets the bottom 8-bits to zero when the coefficient is set to one or zero.

The output from the Exclusive OR circuit is passed to the adder circuit DB, HB, IB and IE where scaled data from channel B is added. The top 8-bits of data from this adder are clocked through the register CB and passed to the Data Select card. The bottom 8-bits from the adder are clocked through the pipe line register BC then passed to the Buffer Store.

(c) CHANNEL B DATA PATH

Data from channel B's selector circuit is clocked through the register HE and passed to the Multiplier LE, where the data is scaled by the coefficient held in the computer loaded register ND. The scaled 16-bit data produced is passed to the adder circuit DB, HB, IB and IE, where scaled A channel data is added. The register OE provides the data bypass path and NF sets the bottom 8-bits to zero when the coefficient is set to one or zero.

(d) CHANNEL C DATA PATH

Data from channel C's selector circuit is clocked through the register GC, when enabled, so that Channel C data can be added to channel A data by the adders IB and IE.

Channel C data can be enabled through the buffer HD to address the coefficient RAMs JA, KA and IC. These RAMs are written with Chroma or Luma keying coefficients from the computer bus via the register ID. The coefficients, when addressed from the channel C, are passed directly to the channel A Multiplier LF via the registers KD and LD. They are also inverted by MA, JC, NA, KC and NC, and passed to the channel B Multiplier LE via the registers LD and MD to provide the 2's complement value.

(e) COMBINER BUS

The combiner bus connects all 4 Combiner cards via bi-directional buffers. This allows data from any source on any satellite Combiner card to be passed to any other satellite to provide the Chroma and Luminance keying facilities.

(f) COMPUTER BUS DECODE

The system computer bus is buffered by DA, BA and AA, and decoded by the Prom CA and the PALs BB and FA to produce the clocks and enable for the computer controlled circuitry on this card. The control register circuit CC, DC, EB, EC, FB and FC, and the register LA are loaded from the system computer bus with the function that is to be performed by the Combiner card.

FIGURE 4.23.1 17732B COMBINER BLOCK

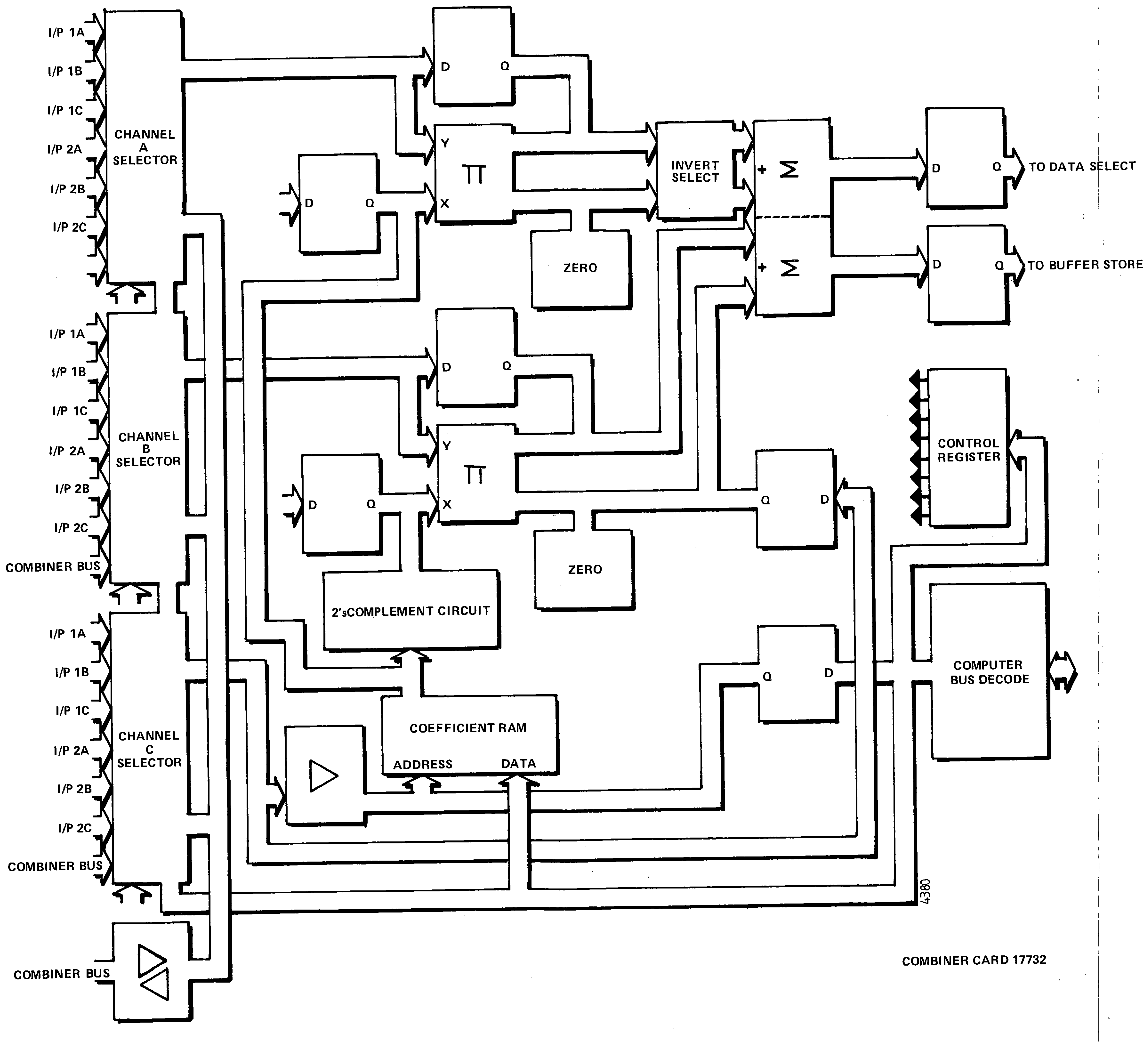
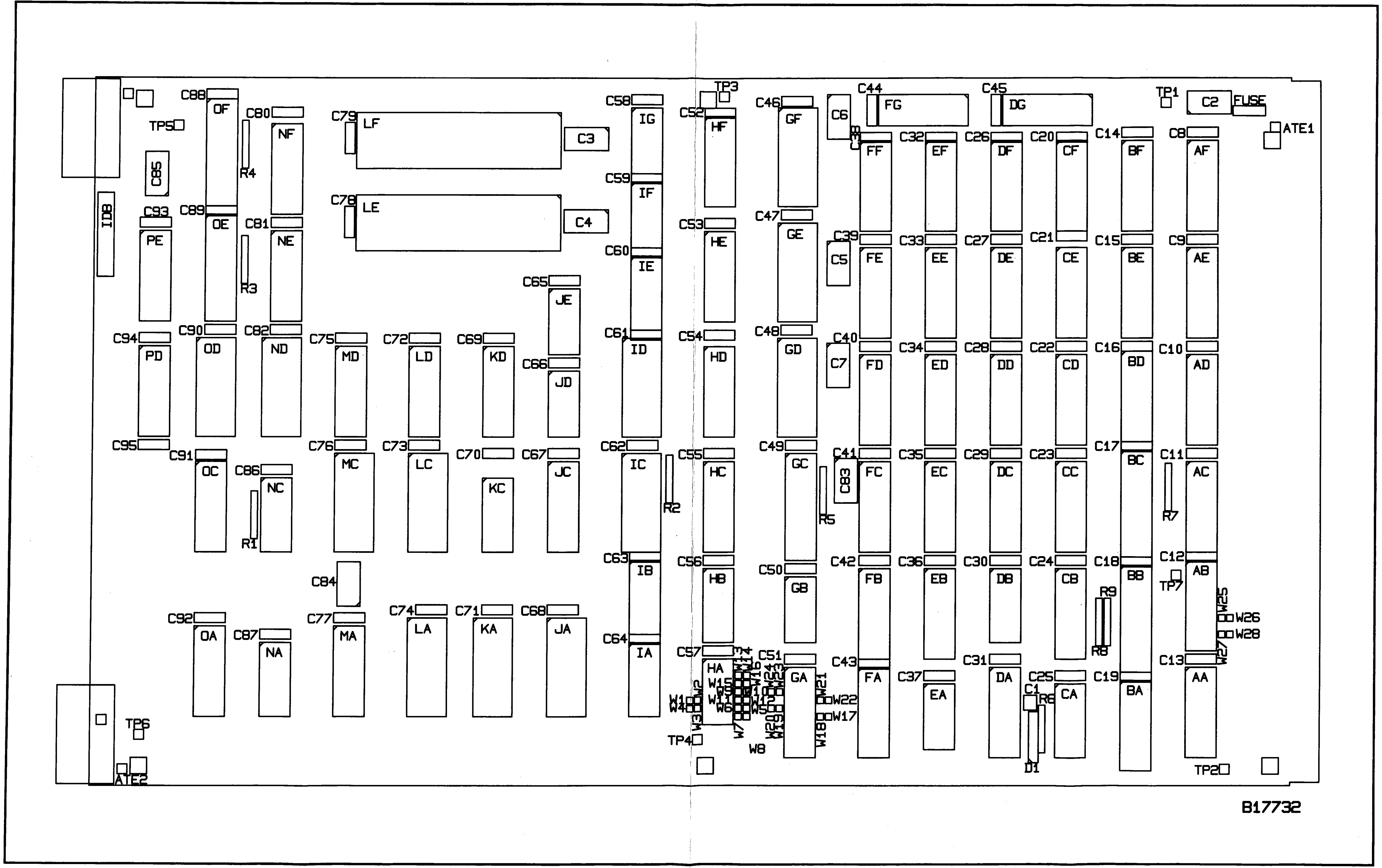
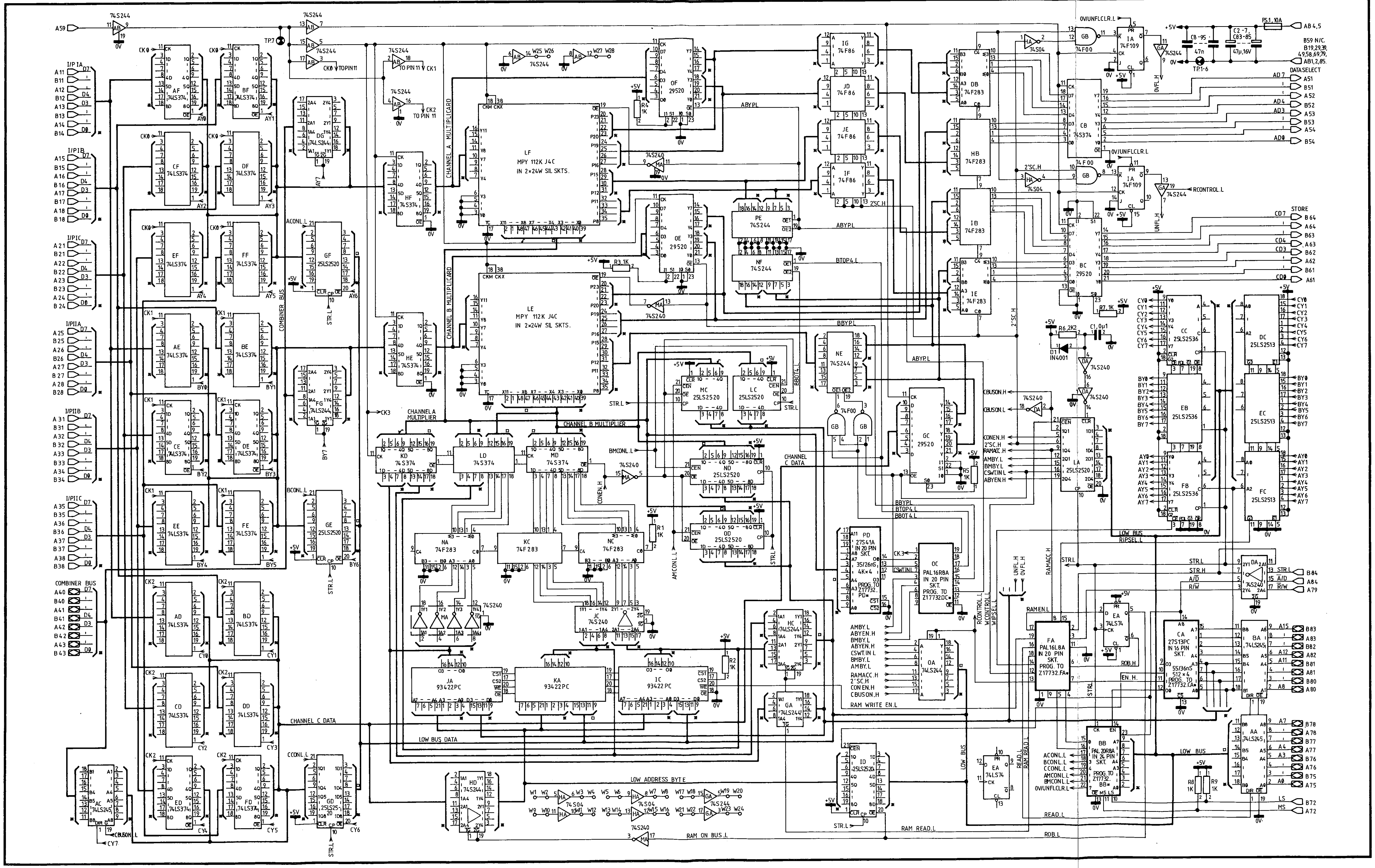


FIGURE 4.23.2 17732B COMBINER LAYOUT



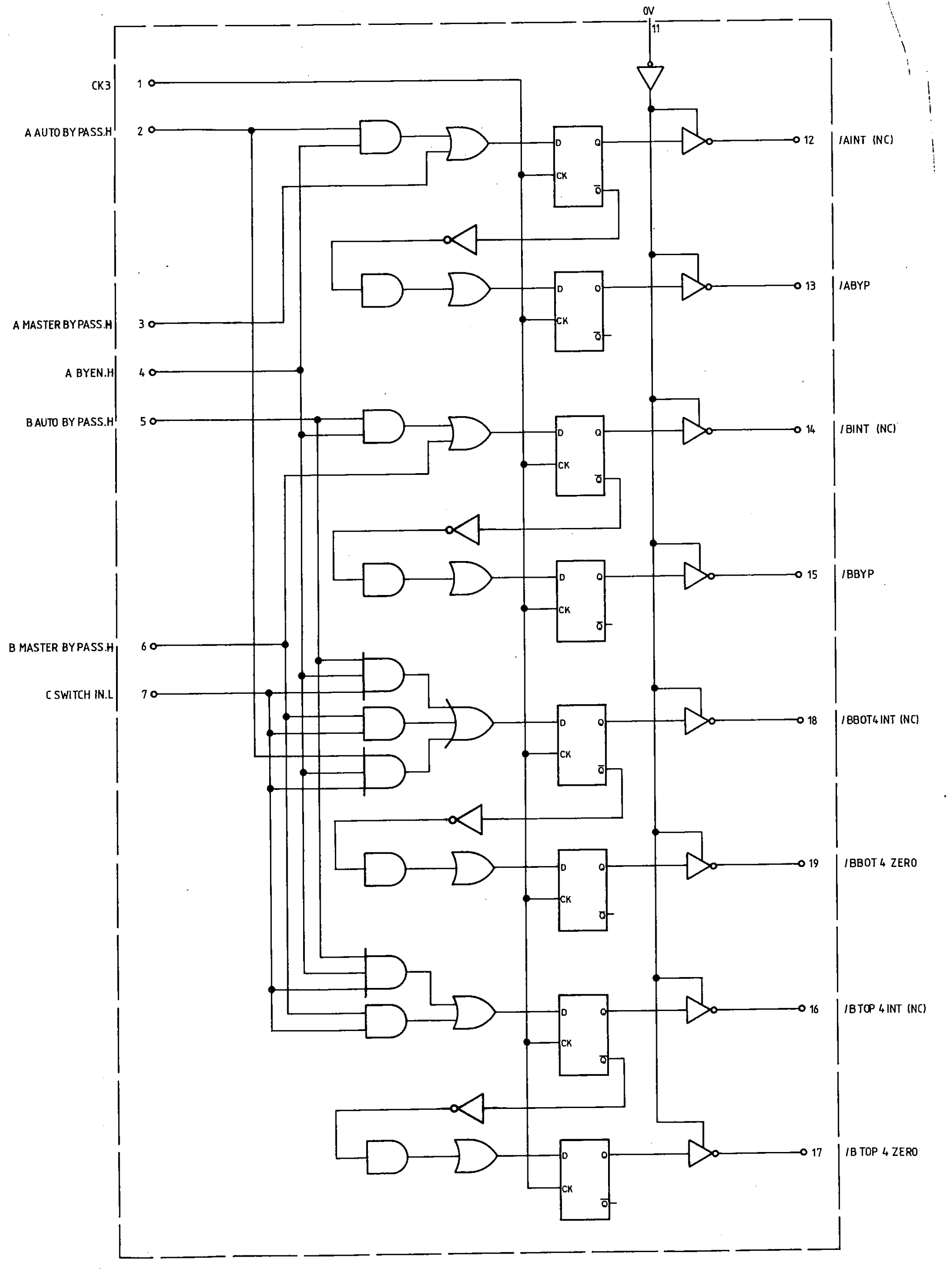
(4,23B)
FIGURE 4.23.3 17732B COMBINER CIRCUIT 1



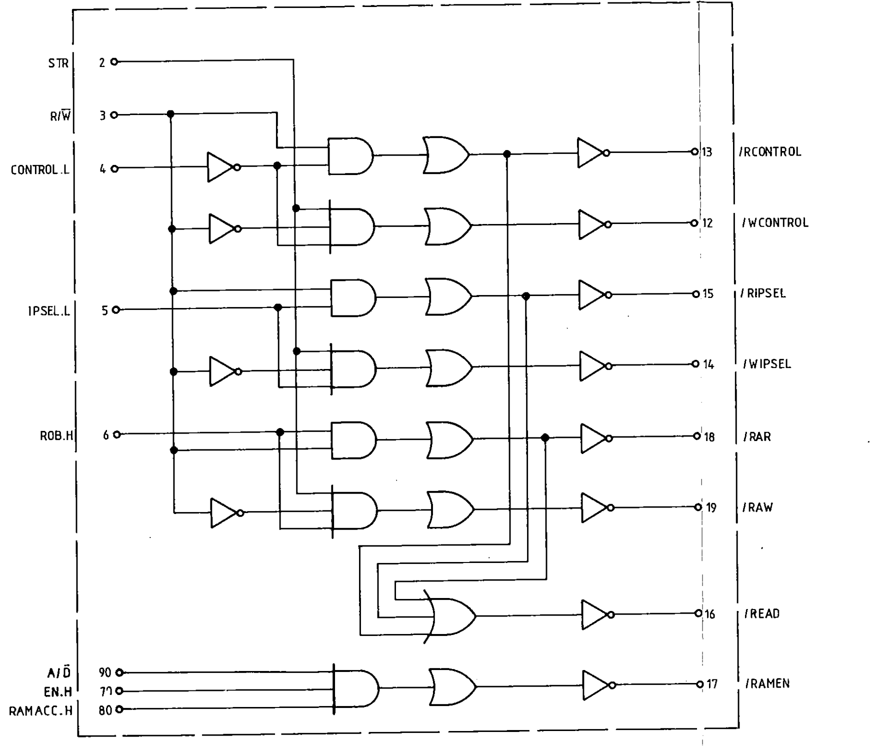
(4,23B)

FIGURE 4.23.4 17732B COMBINER CIRCUIT 2

PAL 16R8A 17732A.0CA (HYCBYC.PAL)



PAL 16L8A 17732A.FAA (HYCRW.PAL)



HARDWIRED SATELLITE ADDRESS			ADDRESSES WHICH WILL ACTIVATE ONE OF EIGHT PAL OUTPUTS.													
SATELLITE	MS	LS	A7	A6	A5	A4	A7	A6	A5	A4	A7	A6	A5	A4	EN	A/$\overline{D}$
T.L.	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1
T.R.	0	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1
B.L.	1	0	0	0	0	0	0	1	0	1	0	0	1	0	1	1
B.R.	1	1	0	0	0	0	0	1	1	0	0	0	1	0	1	1

NB. 'EN' AND 'A/$\overline{D}$' MUST BE HIGH TO ENABLE ANY OUTPUT

ANY OF THE ABOVE STATES WILL ENABLE PAL 20R8A. 17732A.BBA (HYC DEC.PAL) TO DECODE ONE OF EIGHT OUTPUTS FROM A2, A1, A0 (MSB - LSB)

PROM ADDRESS DECODER 17732A.CAA. (HYC BEN.HEX)

OUTPUT \ INPUT	A8	A7	A6	A5	A4	A3	A2	A1	A0	
$O_0 = 1$	1	0	0	0	1	0	1	1	0	0 ELSEWHERE
$O_1 = 1$	1	0	0	0	1	1	0	0	0	0 ELSEWHERE
$O_2 = \overline{O_1} = 0$	1	0	0	0	1	1	0	0	0	1 ELSEWHERE

12 BIT (FFFH) BYPASS DETECTOR. PROM 17732A.PDA (HYC 12B.HEX)

	OUTPUT \ INPUT	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
17732A.PDA 12	A BYPASS.H O_0=1	1	1	1	1	1	1	1	1	1	1	1	1	0 ELSEWHERE
BIT BYPASS DETEST	B BYPASS.H O_1=1	0	0	0	0	0	0	0	0	0	0	0	0	0 ELSEWHERE

INPUT/OUTPUT TIMING CARD 200374YA

4:24:1 Function

There are two Timing cards within the system; one on the input (Write) side of the system and one on the output (Read) side of the system. Their function is to produce the necessary reference locked timing signals, and U and V subcarriers for the system.

The card can be divided into the following operational parts:

Sync Pulse separation

Timing signal generation

Digital subcarrier generation

4:24:2 Circuit Description

(a) SYNC PULSE SEPARATION

The locking reference video signal is terminated, A.C. coupled and buffered, by the amplifier circuit TR9 and QC. The buffered video is passed, via the low pass filter to the sync separator circuit, and via the Chroma peaking amplifier circuit TR3 to the demodulator circuit of the burst locked loop.

The low pass sync separator Luminance is amplified by the current amplifier circuit RG and TR41, and passed to the sync sampler circuit TD and TR5, the black level sampler circuit TC and TR6 , and the comparator circuit TB.

The voltages produced by the sampler circuits are buffered by the OP AMP RC, and summed to produce a voltage equivalent to the 50% level of the sync pulse on the comparator TB.

The TTL sync pulses produced by TB are passed to the monostable TA and the latch SB, which provide the equalizing pulse "time out" signal for the field separator. The circuit consisting of the comparator TB, the diodes D4 and D5, and the resistors R20, 21, 34 and 18, generates a compensating voltage dependant on the average signal level.

The line drive signal produced by TA is passed to the Line locked oscillator circuit and the sync sampler monostable TA. The monostable RB produces the black level and burst sample pulses used by the sync separator and the burst locked loop.

The line locked oscillator circuit consisting of the crystal oscillator NA; the phase detector RA; and the loop filters QA and associated circuitry, produces the 13.5MHz line locked system clock. This clock is phase locked to the locking reference video signal.

(b) TIMING SIGNAL GENERATION

The horizontal counter circuit LA, KA and KB produces a picture point count locked horizontally to the locking reference video. This count is passed to the H phase adder circuit FA, HA and HB, where the value held in the computer loaded registers EB and FB is adder. The output from this adder is passed to the prom GB, which produces the appropriate horizontal timing signals. The outputs from this prom are clocked through the register GE into the combiner proms DC and FF. These proms combine the horizontal and vertical timing signals to produce various composite timing signals.

The vertical counter circuit GG, FG and EG produces a line count locked vertically to the reference locking video. This count is passed to the prom HG, which produces the appropriate vertical timing signals. The outputs from this prom are passed to the combiner proms DC and FF, where they are combined with the horizontal timing signal. The outputs from these proms are then clocked through the registers CC and EF, buffered by BC, and passed to various cards within the system.

(c) SUBCARRIER GENERATION (Digital Path)

The picture point count from LA, KA and KB, and the line count from GG, FB and EG are passed to the phase angle proms IA and JA, and the 25Hz proms JG and IG (PAL only). The phase angle produced by IA and JA is clocked through the registers IB and JB into the offset adder circuit LC, IC and JC. The output from this adder is passed to the adder circuit KF, IF and KC, where the accumulated phase error from the accumulator circuit JF, MF, LG, MG, LF and KG is added.

The phase corrected count from the adder circuit KF, IF and KC is clocked through the registers HE and HC into the reference subcarrier proms LE and KE, and the S phase adder circuit EE, FE and EC, where the value from the computer loaded registers CB and DB is added. The output from the S phase adder is clocked through the registers DE, HC and CF into the subcarrier proms AF and BF (for U), and AE and BE (for V). The outputs from these proms are passed to the Chroma Processor card (Input Timing card) or the Coder card (Output Timing card).

(4,24A)

(d) SUBCARRIER GENERATION (Analogue Path)

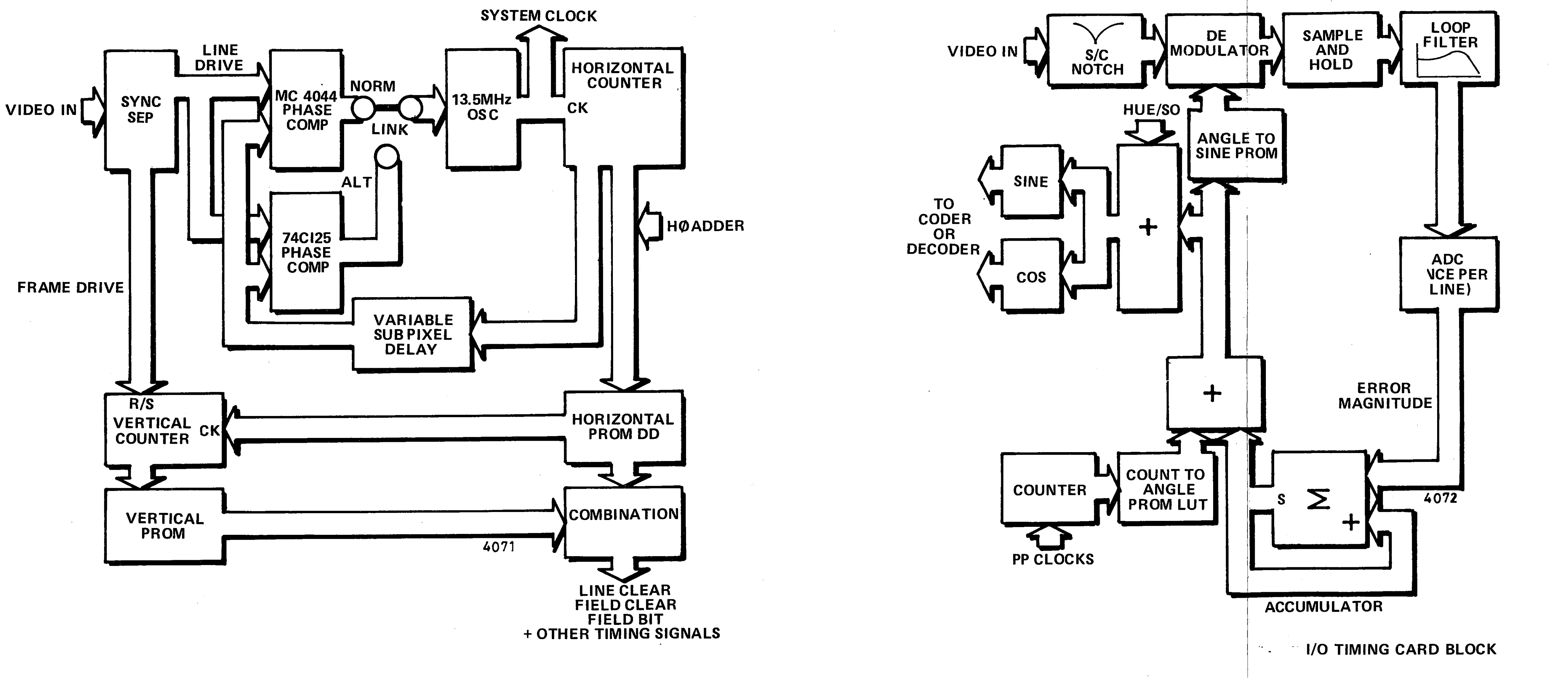
The reference subcarrier data from the proms LE and KE is clocked through the registers ME and HC into the DAC OE, which produces the analogue subcarrier for the demodulator circuit consisting of the multiplier TE and the transformers T1 and T2.

The demodulated reference burst produced by TE is amplified by TF, and sampled by the three sample and hold circuits constructed of TG and RF. Two of the samples are made during the burst position and the other is made during sync duration. The two burst voltages produced are summed and passed to RF (pins 8, 9 and 10) with the voltage produced by the sync sampler circuit.

The output from RF is filtered by the loop filter circuits RF, RG and associated circuitry, then passed to the sample and hold circuit TG, RG and C50, which samples the signal once a line. The sampled phase error from RG is digitized by the ADC OG, then the corresponding error data is passed to the phase error accumulator circuit.

(4,24A)

FIGURE 4.24.1 200374YA I/O TIMING BLOCK DIAGRAM



(4,24A)

FIGURE 4.24.2 200374YA I/O TIMING LAYOUT

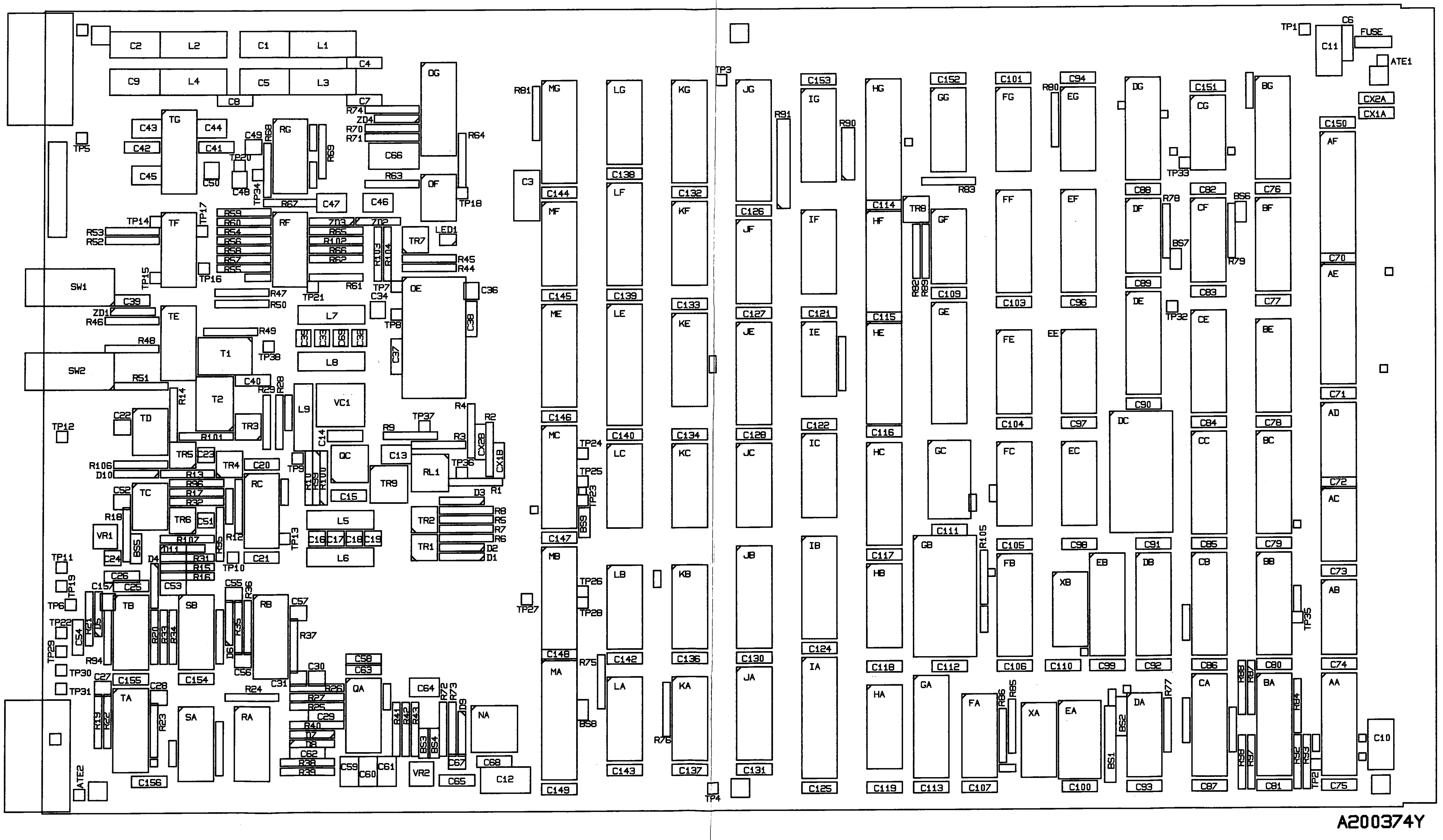
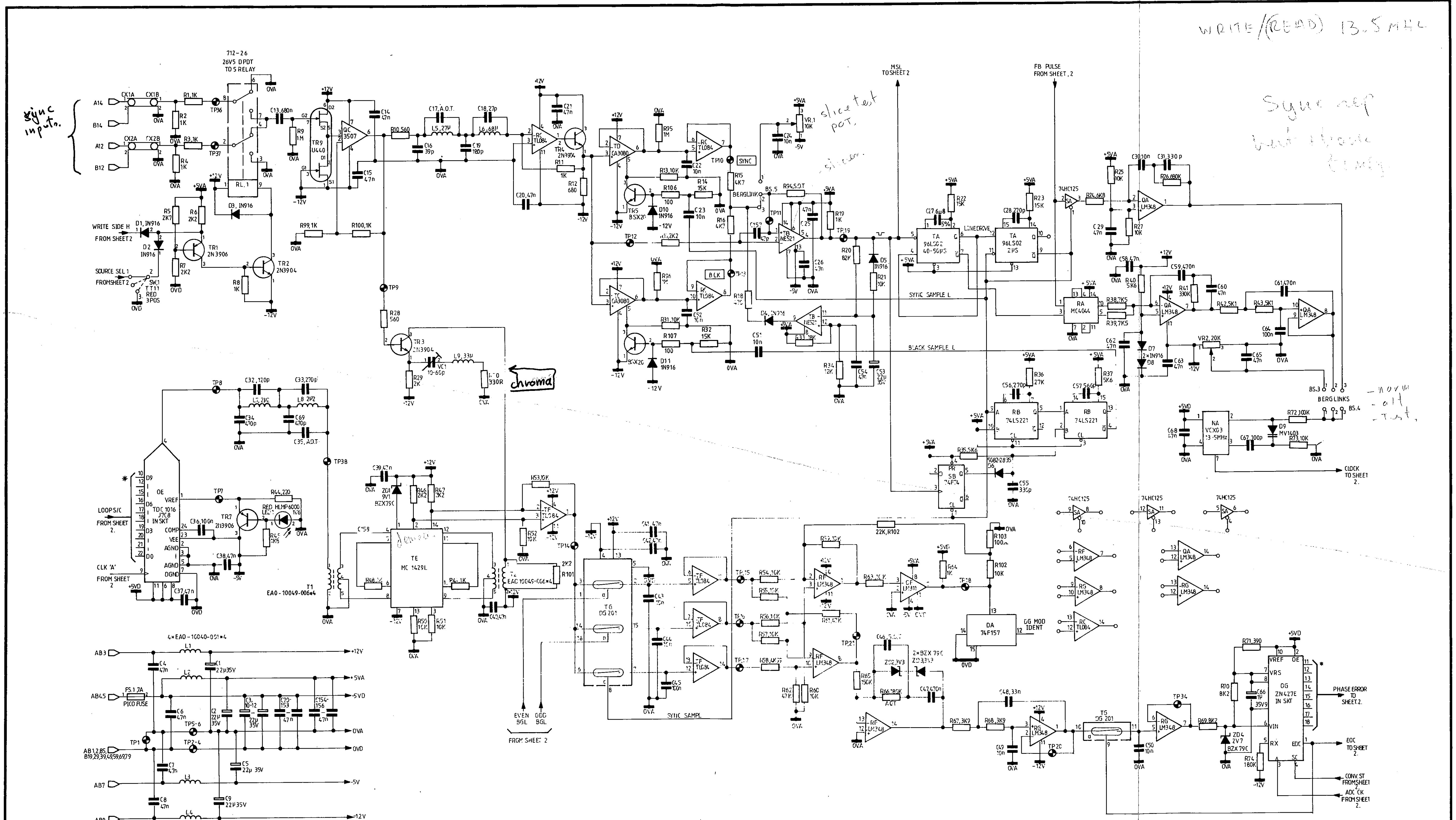


FIGURE 4.24.3 200374YA I/O TIMING CIRCUIT 1



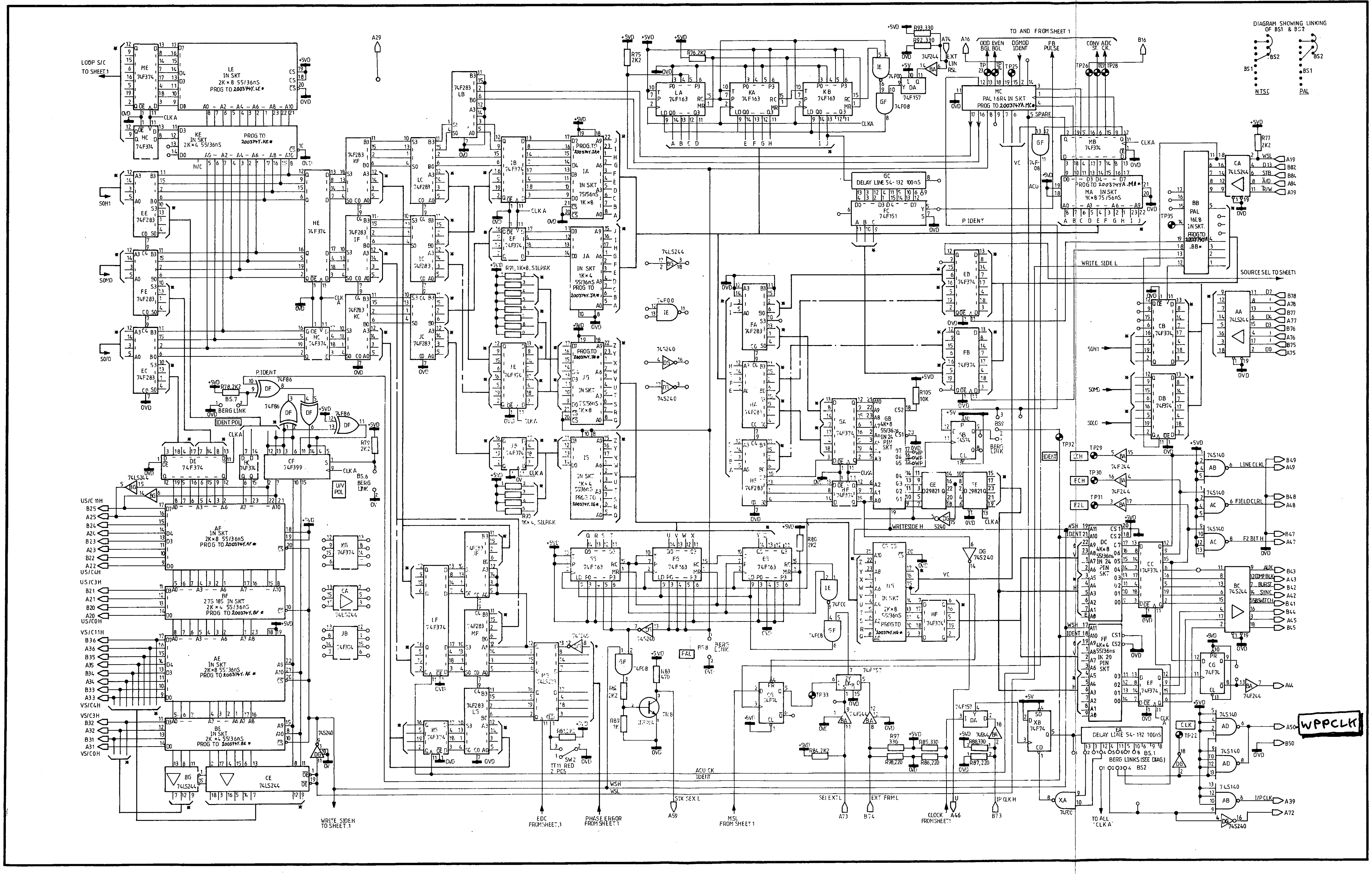
IC POWER CONNECTIONS

TYPE	-12V	-5V	0VD	0VA	+5V	+12V
ZN427E				9	10	
LM 311		4			8	
TDC 1016J		23	7	2,3,5	6	
LH 5033	5					1
LM348&TL084	11					4
MC 1495L	7					
CA 3080	4					7

TYPE	-12V	-5V	0VD	0VA	+5V	+12V
14 PIN DIL				7	14	
16 PIN DIL				8	16	
18 PIN DIL				9	18	
20 PIN DIL				10	20	
24 PIN DIL				12	24	
NE 521		13		7	14	
DG 201	4			5		13

(4,24A)

FIGURE 4.24.4 200374YA I/O TIMING CIRCUIT 2



AUDIO PROCESSOR 2003716B

4:25:1 Function

The function of the Audio Processor card is to provide an audio scratch track for the system. This is used to store the audio track associated to a particular Video clip.

The card accepts a standard audio signal as its input, and provides an output signal synchronous with the processed output Video clip being generated. The card processes the audio signal in digital form, allowing up to 120 seconds to be stored in the 1 Mbit DRAM section on the card.

4:25:2 Circuit Description

(a) ANALOGUE AUDIO INPUT PATH

The analogue Audio input signal from the "Audio In" connector, on the top rear I/O panel, is terminated by the card into the required matched input impedance. The balanced signal is then AC coupled and buffered by the amplifier stage formed by WB and associated components.

The output from the amplifier stage is passed to the computer controlled attenuator formed by the DAC UB (Logarithmic function) and the amplifier UC. The attenuation factor is generated by the system computer and held in the register MA.

The attenuated output signal produced by UC is clamped by Diodes D5 and D6, which clip signals greater than +/- 4 Volts. The signal is then passed though the 2 stage 10 pole filter circuit formed by SC, PB and the amplifier RB. The filter signal is passed through the Sample & Hold circuit SD before the sampled signal is digitized by the ADC PC to provide 16-bit data.

The analogue input is also buffered by the amplifier stages WC and associated components into the bar-graph VU circuit formed by I1C and the LEDs 1 to 10. This circuit is used to monitor the amplitude of the input signal.

(b) DIGITAL AUDIO PATHS

The 16-bit audio data produced by the ADC PC is clocked through the registers KB and MF into the Dynamic RAM section of the card. The data is then written to the RAM location setup by the Row and Column addresses.

Computer generated data can also be written into the RAM section via the register LI and JF, controlled by the PAL BD.

The data read from an addressed location is clocked through the registers LB and LD into the DAC NC, which produces the output analogue audio signal.

The output of the RAM can be read by the system computer via the registers MI and KF, controlled by the PAL BD.

(c) ANALOGUE AUDIO OUTPUT PATH

The 16-bit audio data from the registers MB and MD (audio bypass path) or the registers LB and LD (output from RAM section) is converted to analogue by the DAC NC. The audio signal produced is filtered by the 2-stage 10-pole filter circuit formed by NA and RA, and the amplifier PA. The filtered signal is amplified by UA and associated components then attenuated by SB and SA, controlled by the computer loaded register LA.

The attenuated signal generated by SA is buffered by the amplifiers UA and WA to provide the balanced "Audio Out" signal.

(d) RAM ADDRESSING

The Row and Column addresses for the dynamic RAMs on the card are generated by computer controlled counter circuits. These provide independent audio and computer addresses for the RAM section, which allows simultaneous access to the data stored in the RAMs.

The audio address counter circuit BH, CH, CI, DI, CF and DF is clocked by sample rate clocks and loaded with the value held in the computer loaded registers AF, BI and BF. The incrementing binary count produced is passed through the buffers DH, EI and EF into the buffers KI and KH. These are alternately enabled to provide the Row and Column addresses for the dynamic RAMs.

The computer address counter circuit HH, IH, GI, HI, FD and GF is clocked by computer rate clocks and loaded with the value held in the computer loaded registers GH, EH, FI and FH. The incrementing binary count produced is passed through the buffers JH, II and IF into the buffers KI and KH. These are alternately enabled to provide the Row and Column addresses for the dynamic RAMs.

The RAS and CAS signals for the RAMs are generated in Audio access, Computer access and Refresh cycles. The arbitration over which cycle is to occur first is determined by the control PAL HB and the latches EA, FB and JB which process cycle requests from these sources. The 16MHz oscillator XL1 provides clocks for the arbitration circuitry, which are used to request refresh cycles.

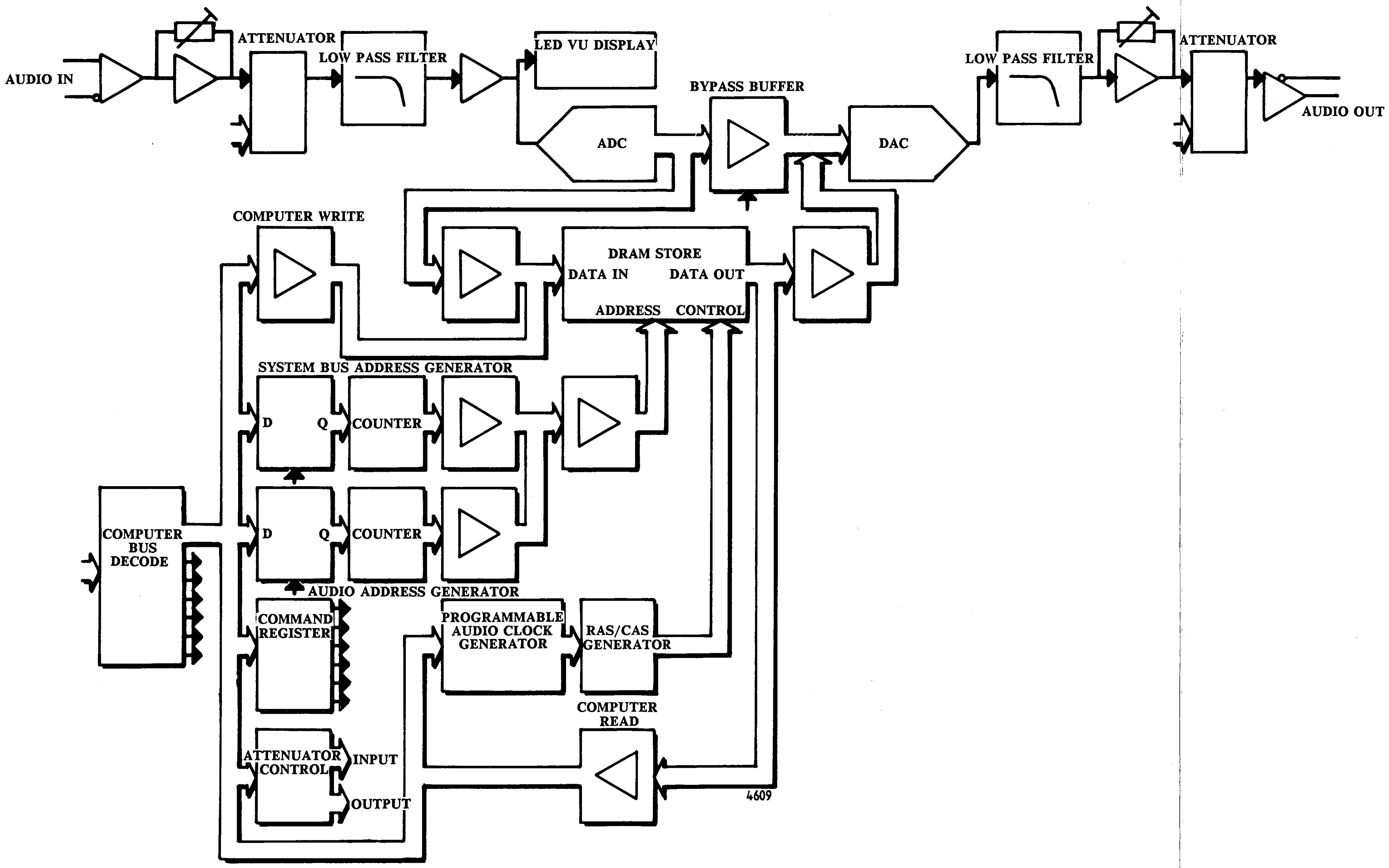
The PAL HB instigates a store cycle by triggering the Latch IC. This action passes a pulse edge through the delay lines IC and JC. The delayed taps are then combined by ID and JD to generate to the correctly timed RAS and CAS signals. These are passed to the PAL LH, which routes them through to one of the 4 RAM stripes determined by decoding the 2 most significant address bits.

(e) COMPUTER BUS DECODE

The system computer bus is buffered by AA, AD and AB then decoded by the PALs BB, BD, CD and FF. These PALs decode the computer commands to provide the clock and enable signals for the computer controlled circuitry on the card.

The PAL BB decodes the card addresses, which allows the PALs BD, CD and FF to receive data of the system bus. The PAL BD decodes bus transfer operations. The PAL CD controls the computer loaded registers AF, BI, BF, GH, EH, FI and FH. The PAL FF controls the computer loaded registers MA and LA, which hold the attenuator coefficients for the analogue circuitry. The computer loaded register DD is the card function register, and controls the operation of the card.

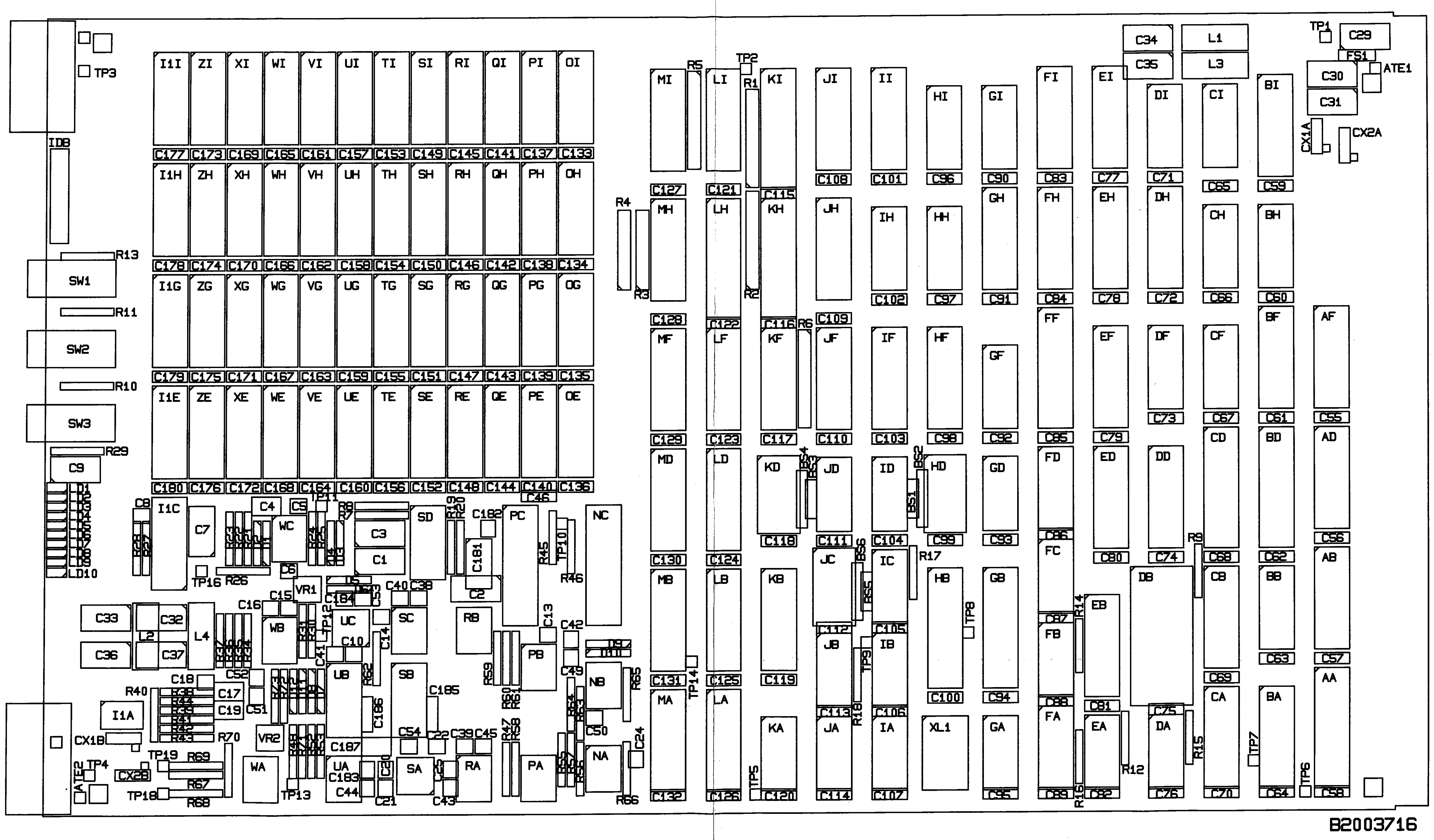
(4,25B)
FIGURE 4.25.1 2003716B AUDIO PROCESSOR BLOCK



2003716 AUDIO PROCESSOR

available.
120 secs

(4,25B)
FIGURE 4.25.2 2003716B AUDIO PROCESSOR LAYOUT


TP3
I1I ZI XI WI VI UI TI SI RI QI PI OI
C177 C173 C169 C165 C161 C157 C153 C149 C145 C141 C137 C133
I1H ZH XH WH VH UH TH SH RH QH PH OH
C178 C174 C170 C166 C162 C158 C154 C150 C146 C142 C138 C134
I1G ZG XG WG VG UG TG SG RG QG PG OG
C179 C175 C171 C167 C163 C159 C155 C151 C147 C143 C139 C135
I1E ZE XE WE VE UE TE SE RE QE PE OE
C180 C176 C172 C168 C164 C160 C156 C152 C148 C144 C140 C136
C46
IDB
R13
SW1
R11
SW2
R10
SW3
R29
C9
D1 D2 D3 D4 D5 D6 D7 D8 D9 LD10
C8 I1C C7 C4 C5 TP11 R8 R7 WC C3 C1 SD R19 R20 C182 PC NC
C6 TP16 R26 C181 R45 TP10 R46 C2
VR1 C15 C16 C184 C40 C38 UC SC RB C13 C42
C33 C32 L2 L4 WB TP12 C10 C14 PB
C36 C37 C41 UB SB R62 R59 C49 NB R65
C18 C52 C17 C19 C51 C186 C185 R60 R61 C50 C24
R40 I1A R70 VR2 C187 C54 C22 C39 C45 R47 R58
CX1B TP4 TP19 R69 ATE2 CX2B WA UA C183 C30 SA C25 RA PA NA
TP18 R67 R68 TP13 C44 C21 C43 R66
MI R5 LI TP2 R1 KI JI II HI GI FI EI DI CI BI
C34 C35 L1 L3 TP1 C29 FS1 C30 C31 ATE1 CX1A CX2A
C127 C121 C115 C108 C101 C96 C90 C83 C77 C71 C65 C59
R4 MH LH KH JH IH HH GH FH EH DH CH BH
R3 R2 C128 C122 C116 R6 C109 C102 C97 C91 C84 C78 C72 C66 C60
MF LF KF JF IF HF GF FF EF DF CF BF AF
C129 C123 C117 C110 C103 C98 C92 C85 C79 C73 C67 C61 C55
MD LD KD R54 R53 JD ID BS2 BS1 HD GD FD ED DD CD BD AD
C130 C124 C118 C111 C104 C99 C93 C86 C80 C74 R9 C68 C62 C56
MB LB KB JC BS6 BS5 IC R17 HB GB FC R14 EB DB CB BB AB
C131 TP14 C125 C119 C112 C105 TP8 C87 TP9 C63 C57
JB IB FB C100 C94 C88 C81 C75 C69
MA LA KA JA R18 IA XL1 GA FA EA DA R15 CA TP7 BA AA
TP5 C113 C106 R12
C132 C126 C120 C114 C107 C95 C89 R16 C82 C76 C70 C64 TP6 C58
B2003716

(4,25B)

FIGURE 4.25.3 2003716B AUDIO PROCESSOR CIRCUIT 1

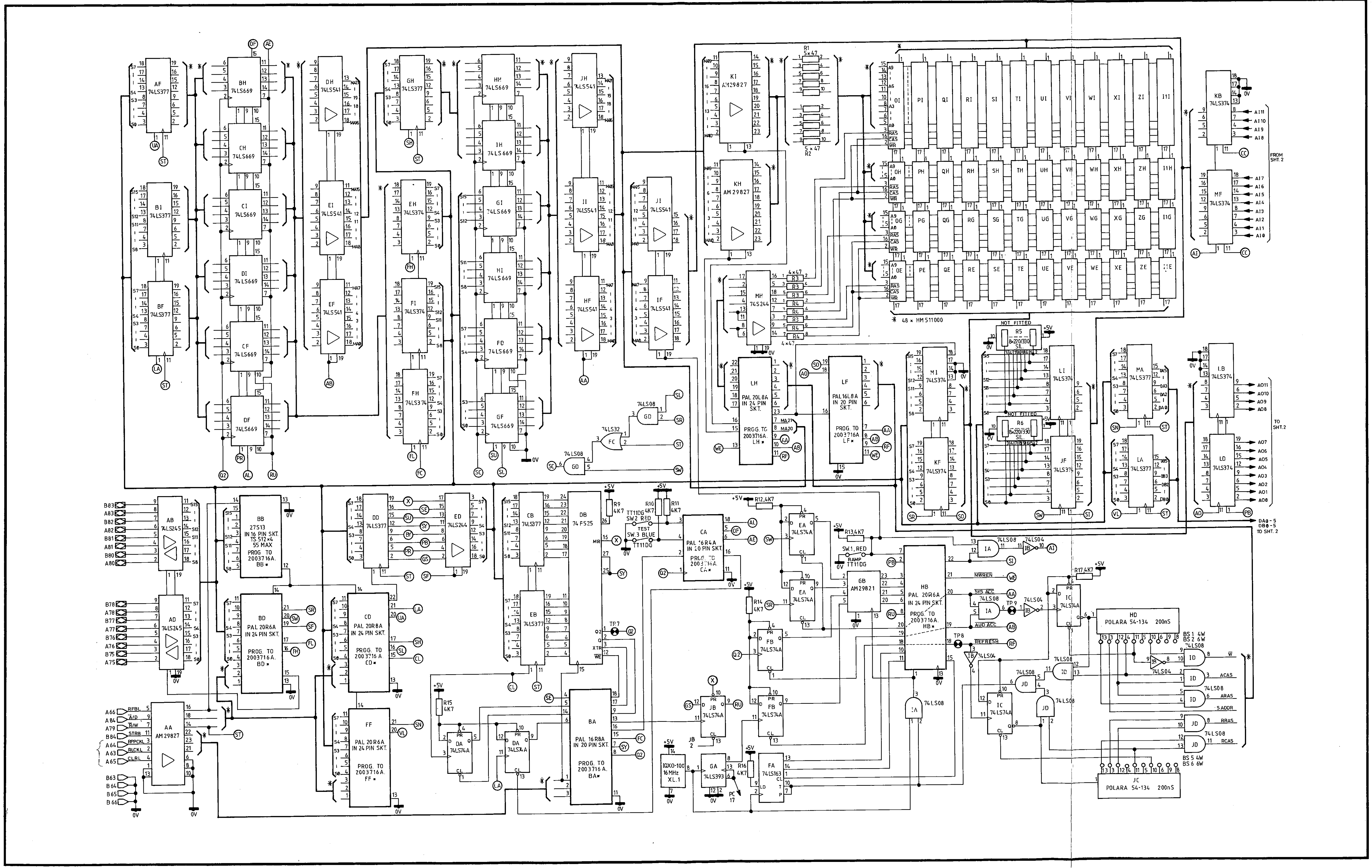
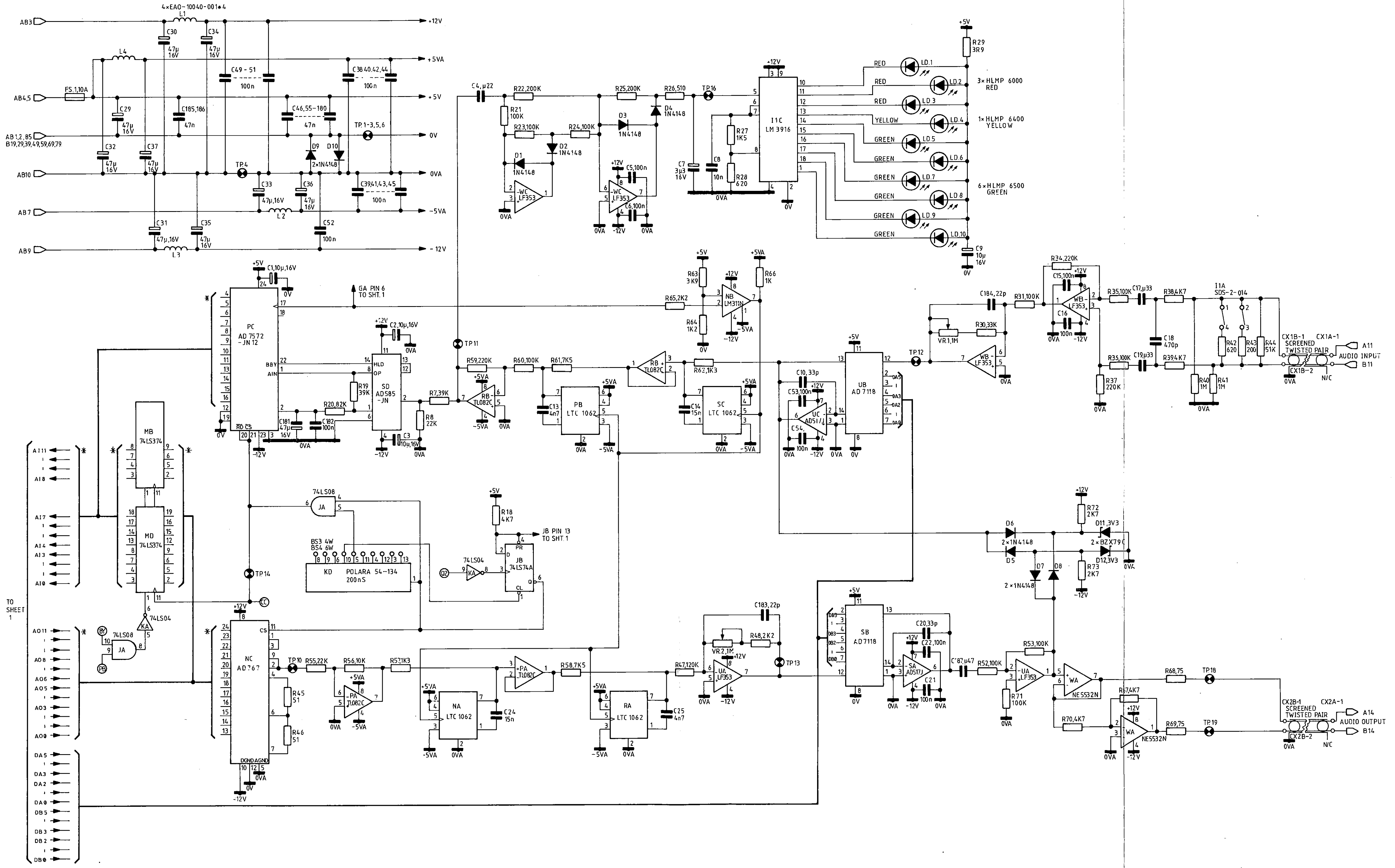


FIGURE 4.25.4 2003716B AUDIO PROCESSOR CIRCUIT 2



IC. POWER CONNECTIONS.

TYPE	-5V	0V	0VA	+5V
14 PIN DIL		7		14
16 PIN DIL		8		16
20 PIN DIL		10		20
24 PIN DIL		12		24
HM 511000		18		9
LTC 1062	3		2	6

TYPE	-12V	-5V	0V	0VA	+5V	+12V
AD 7572			12	3	24	
AD 7118			8	1		11
AD 517J	4					7
AD 585JN	4					11
LM 3916			2	4		3,9
LF 353	(4)	(4)			(8)	(8)

DCR 7700/1 HARRY
INSTALLATION AND SERVICE MANUAL
CHAPTER 5 : CIRCUIT DESCRIPTIONS

This chapter contains the circuit descriptions, the component layouts, and the circuits for the following modules and internally mounted printed circuits boards:

5:1:1 2003724 Harry Interface ____ 339

5:2:1 13356 Over Temperature 2 ____ 343

5:3:1 13360 BNC Screen card ____ 347

5:4:1 200391Y I/O Expander Input card ____ 351

5:5:1 2003988 I/O Expander Output card ____ 357

HARRY INTERFACE CARD 2003724A

5:1:1 Function

The function of this card is to interface the Harry system with the Paintbox system. The Harry system, when connected, provides the Paintbox Input and Output side timing signals and clocks. The card is fitted in the SMD highway of the Paintbox and connects the two systems via two 50-way ribbon cables. This allows data to be transferred to and from the Paintbox processing circuitry and the Harry system.

5:1:2 Circuit Description

(a) LUMINANCE DATA PATHS

Luminance data from the Paintbox highway at the Combiner card is buffered by AE, clocked through the register BE then passed the Harry system via the buffer CE and SKT 1.

Luminance data from the Harry system is buffered by BB, clocked through the register AB and passed the Paintbox Input Timing card.

(b) U/V DATA PATH

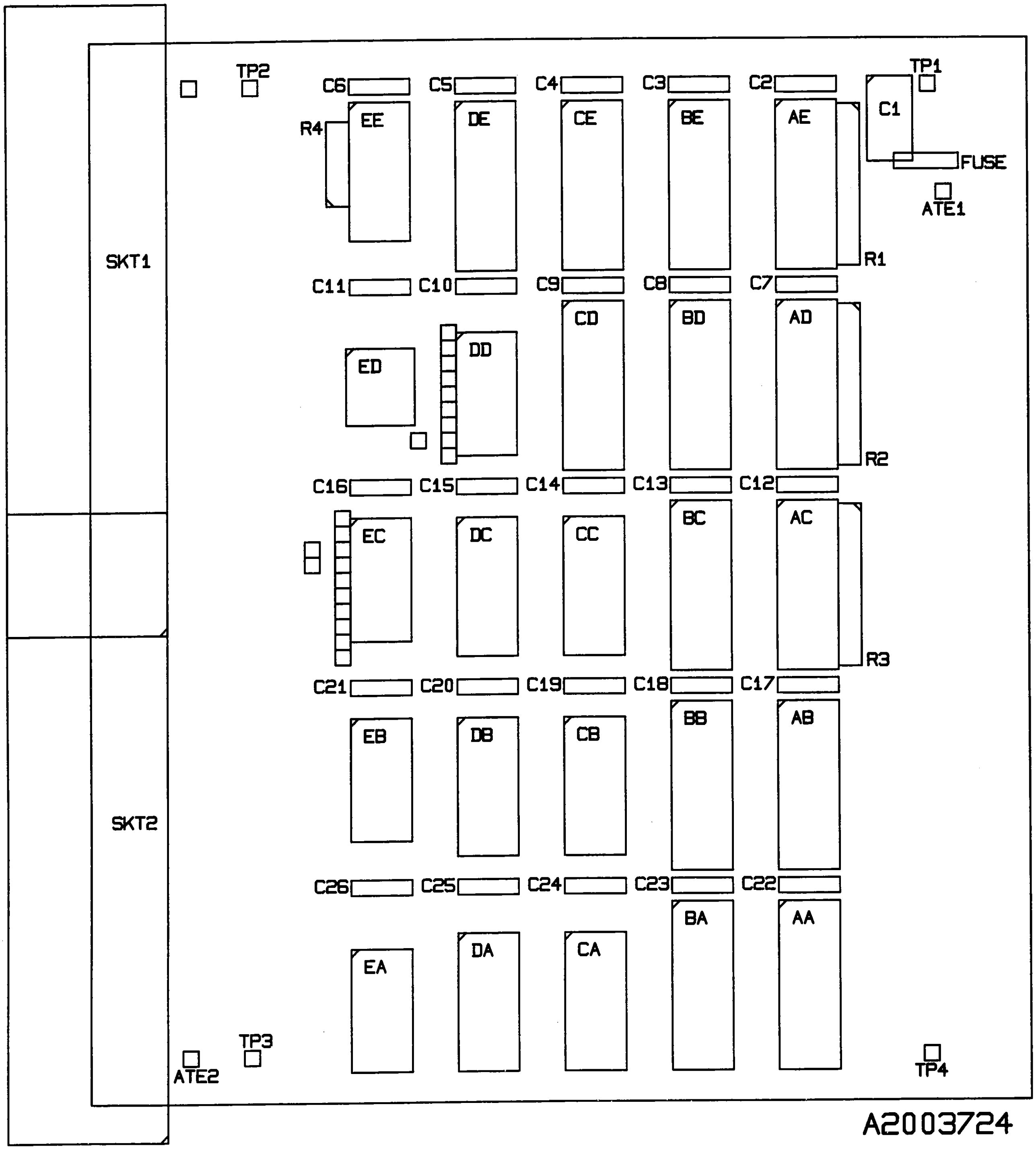
Multiplexed U/V data from the Paintbox highway at the Combiner card is buffered by AD, clocked through the register BD and then passed to the Harry system via the buffer CD and SKT1.

Multiplexed U/V data from the Harry system is buffered by BA, clocked through the register AA and passed Paintbox Input Timing card.

(c) TIMING SIGNAL PATHS

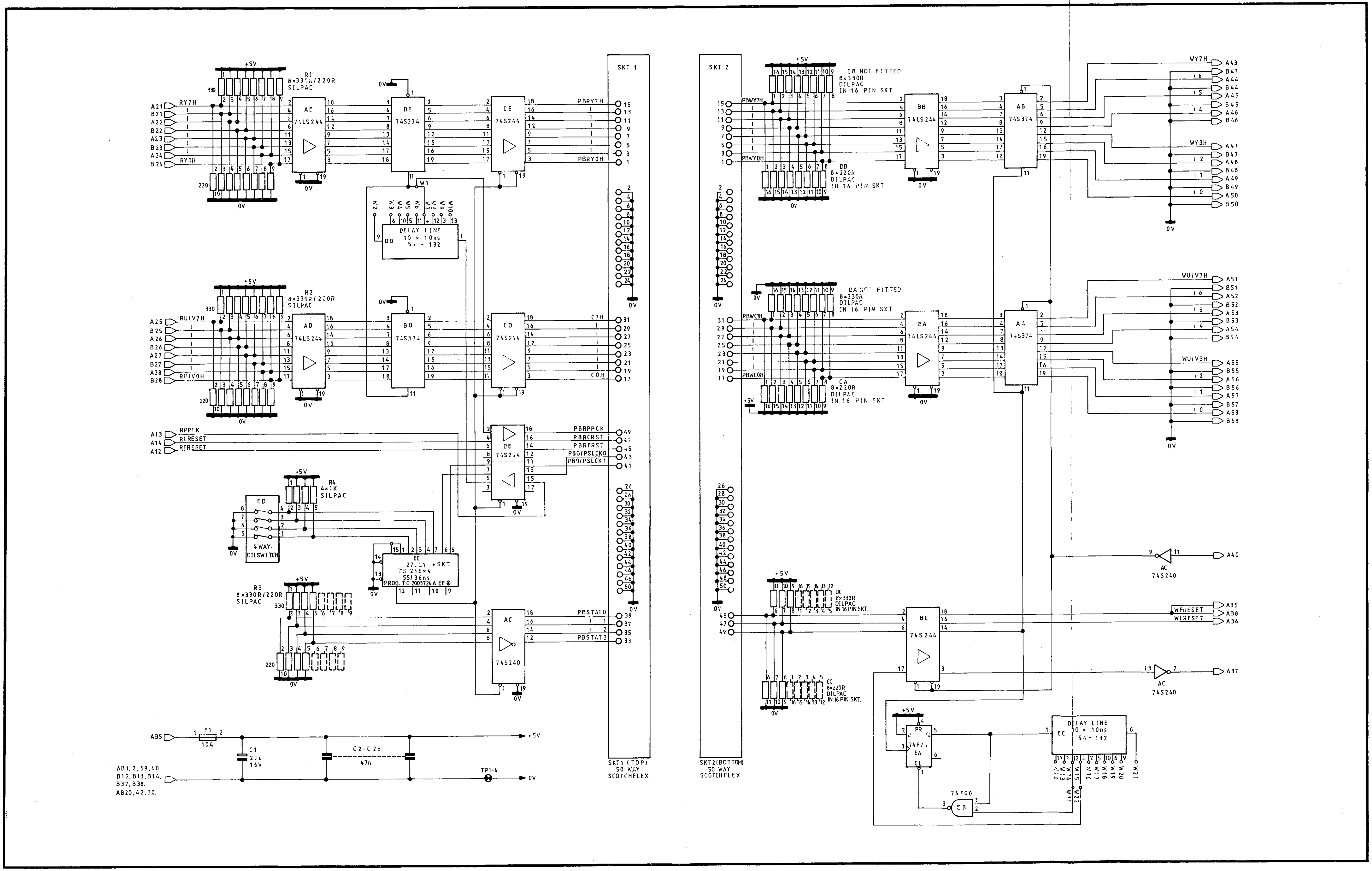
Input side timing signals and clocks from the Harry system are buffered by BC and passed to the Paintbox Input Timing card. Output side timing signals and clocks from the Harry system are buffered by DE and passed to the Paintbox Output Timing card. These timing signals are phase locked to the locking reference video signals of the Harry system.

FIGURE 5.1.1 2003724A HARRY INTERFACE LAYOUT



(5,1A)

FIGURE 5.1.2 2003724A HARRY INTERFACE CIRCUIT



OVERTEMP 2 CARD 13356B

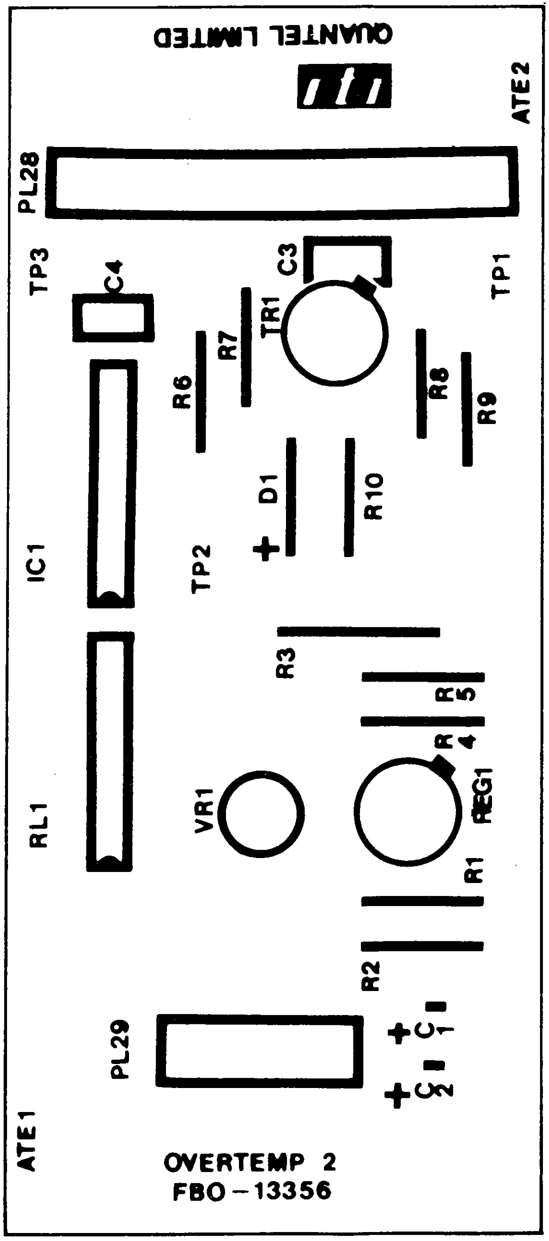
5:2:1 Function

The Overtemp 2 card forms part of the system's over-temperature alarm circuitry. The system's air temperature is measured by the overtemp 1 card mounted within the DCR 7700/1 unit, and measures the temperature of the expelled air. The output from the sensors on the Overtemp 1 card are passed to the Overtemp 2 card mounted in the Power Supply unit, which detects when the system's air temperature exceeds the preset level.

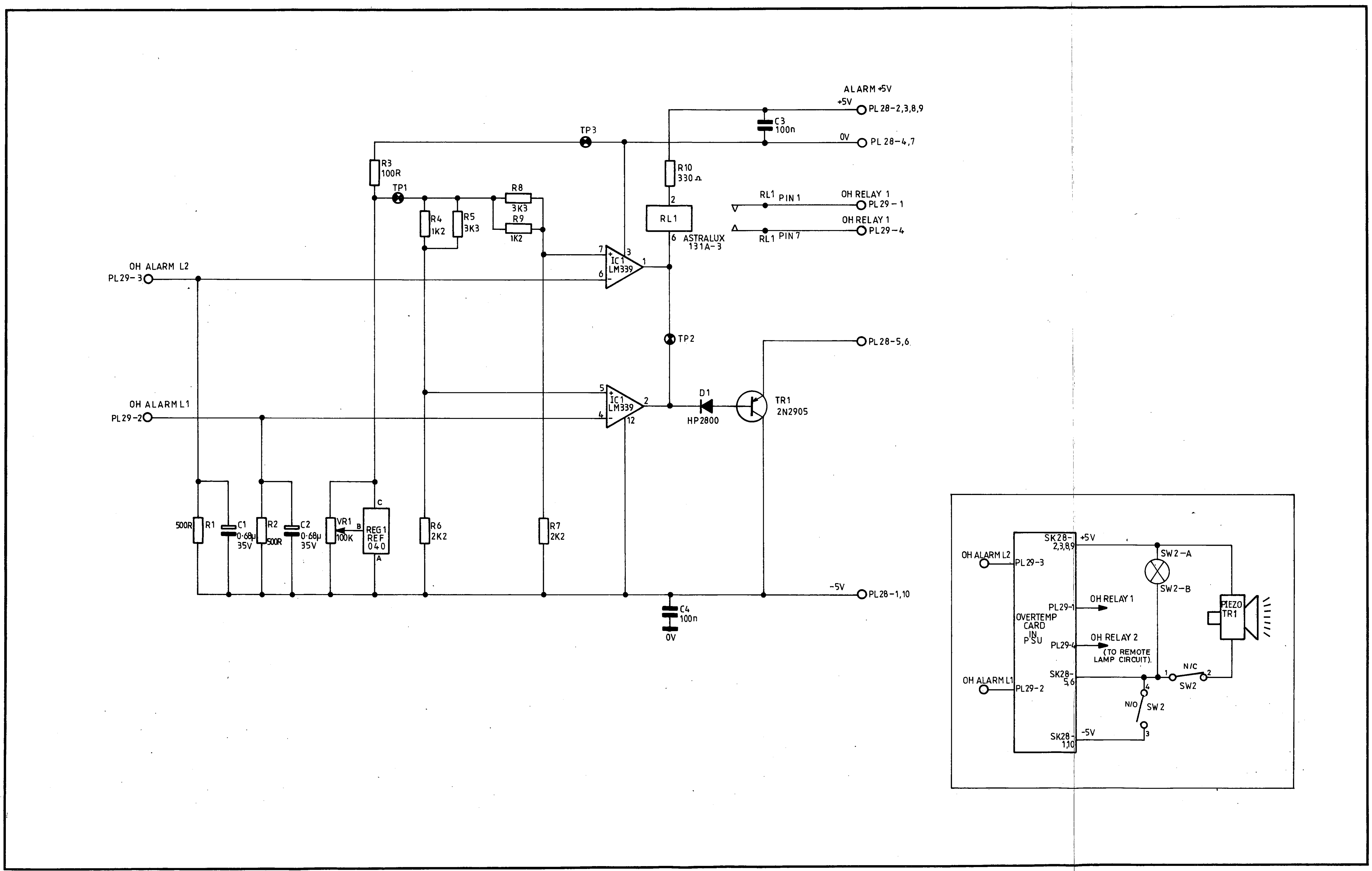
5:2:2 Circuit Description

The sensor output levels from the Overtemp 1 card are fed to the 2 parts of the OP AMP IC 1, which form a comparator circuit. This circuit compares the preset voltage level from VR1 with the sensor input voltages, and turns on TR1 for the remote alarm output and Relay 1 for the PSU alarm.

FIGURE 5.2.1 13356B OVERTEMP 2 CARD LAYOUT



(5,2B)
FIGURE 5.2.2 13356B OVERTEMP 2 CARD CIRCUIT



BNC SCREEN CARD 13360B

5:3:1 Function

The BNC Screen card allows the system's external BNC video signals to be connected to the DCR 7700/1 card highway. This card provides an RFI screen between the system and the external connections. The BNC Screen card also holds the Main Video bypass relay, which is activated by system power failure.

5:3:2 Circuit Description

(a) SYNC IN

The SYNC IN signal is terminated by R5 and AC coupled into the the Base of the emitter follower TR1. The buffered signal is then passed to the Input Timing card as the external locking (RGB Sync) reference.

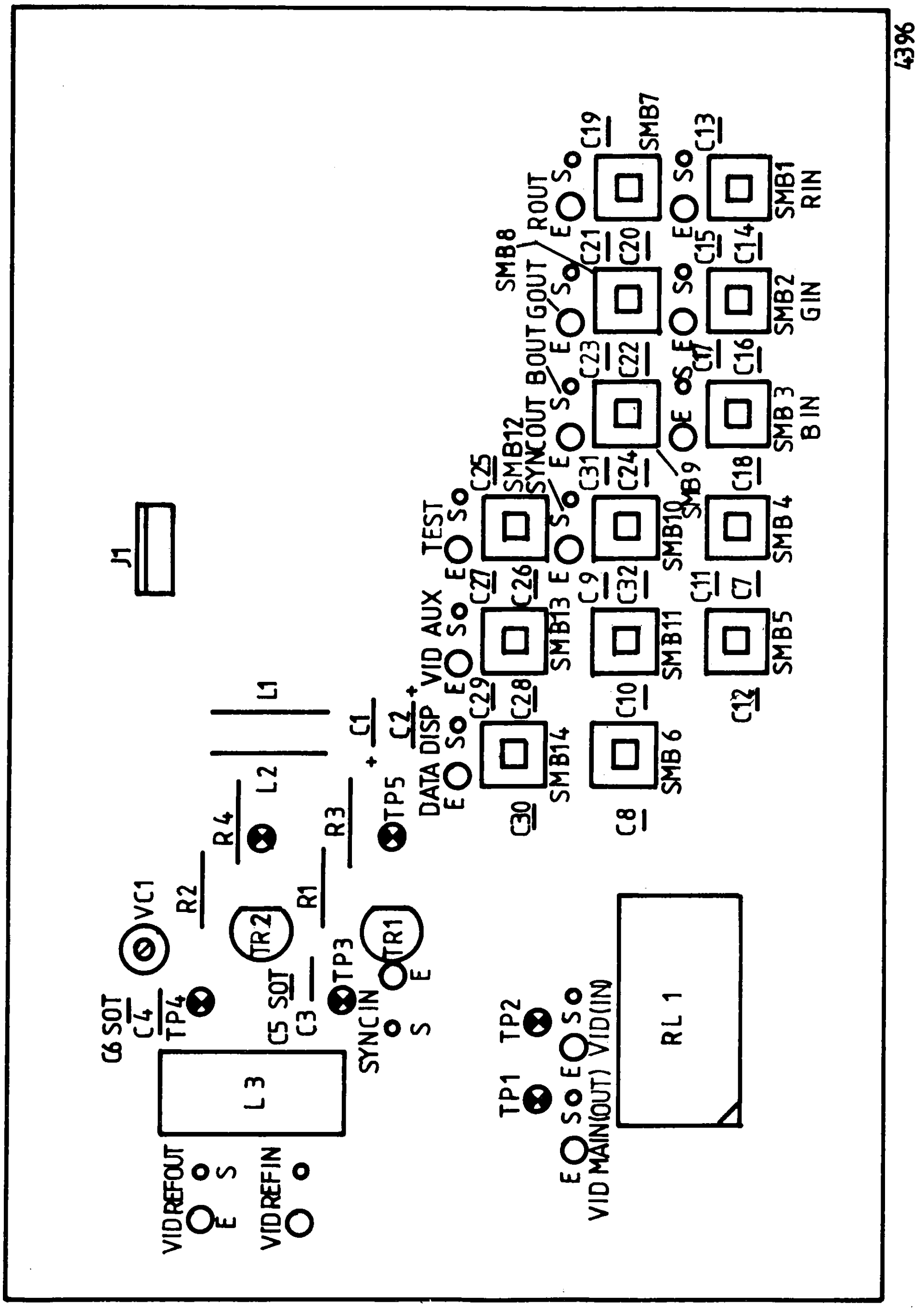
(b) VID REF IN

The VID REF IN signal is passed through the Return loss coil L3 and the centre tap is tuned by C6 and VC1. The tuned signal is AC coupled by C4 into the base of the emitter follower TR2. The buffered signal is then passed to the Output Timing card as the external locking reference.

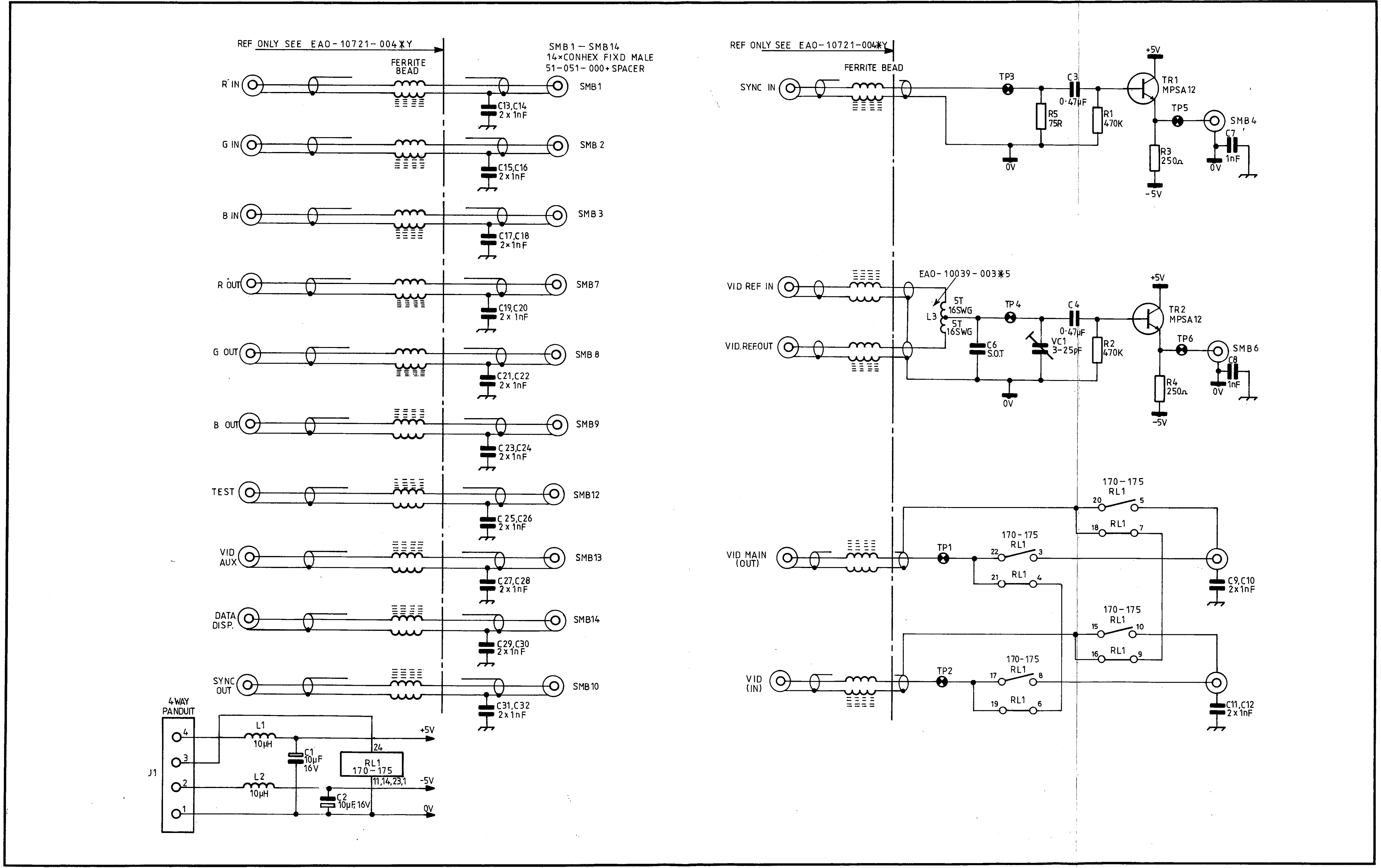
(c) MAIN VID

The Coded input signal is selected by the bypass relay RL1 and passed to the ADC card. The Coded output signal from the Coder card is passed to the bypass relay, which routes the signal to the Main Vid Out socket.

FIGURE 5.3.1 13360B BNC SCREEN CARD LAYOUT



(5,3B)
FIGURE 5.3.2 13360B BNC SCREEN CARD CIRCUIT



I/O EXPANDER INPUT CARD 200391YC

5:4:1 Function

The function of this card is to provide 4 selectable digital video inputs for the system, 2 EBU 601 digital inputs and 2 Quantel standard digital inputs. The card is mounted in the rear of the Harry crate assembly on the inside of the top rear panel (I/O Panel). The card forms a 4 - 1 selector, controlled by the system via the PAL HF.

The EBU 601 video data is transmitted as 8-bit complementary pair ECL at 27MHz sample rate. The data is in multiplexed Y, U and V form providing 4:2:2 samples respectively. The Y component has a 13.5MHz sample rate and the U and V samples both have 6.75MHz sample rates. The 601 data is accompanied by a 27MHz clock which is used to de-multiplex the Y, U and V components

The Quantel Standard Video is transmitted as three 8bit TTL data buses at 13.5MHz sample rate. The Y, U/V and Key components are transmitted separately and are each sampled at 13.5MHz. The Quantel Standard data is accompanied by a 13.5MHz clock, which is used to accurately time data/clock transitions within the system.

5:4:2 Circuit Description

(a) EBU 601 INPUTS

EBU 601 digital video from the "Channel 1" input connector on the top rear panel is passed to the card via the 26-way ribbon connector PL3. The complementary pair ECL data is then buffered by KA to IC and converted to TTL levels by HE and FE. The TTL data produced is clocked through the register EE, whose output is enabled by the PAL HF, to form half of a 2-1 selector circuit.

EBU 601 digital video from the "Channel 2" input connector on the top rear panel is passed to the card via the 26-way ribbon connector PL4. The complementary pair ECL data is then buffered by HA to FC and converted to TTL levels by ID and FD. The TTL data produced is clocked through the register ED, whose output is enabled by the PAL HF, to form half of a 2-1 selector circuit.

The output data from the selected register (EE or ED) is clocked alternately (at 27MHz) into the registers FG (Y component) and EC (U/V component). The Y data and U/V data are then clocked through the registers EG and DA (at 13.5MHz rate) into the pipe-line registers CG and CA, whose effective delay is controlled by the Prom AF. The delayed data is then clocked through the registers BC (Y component) and BA (U/V component) to be passed to the Chroma Proc card.

The TTL 601 data produced at the output of the register EE or ED is decoded by the PAL EF to extract the sync words embedded in the data. The PAL generates various signals, LS (line start), TT (timing next word) and CK (divided clock), and the de-multiplexer signals (YE and CE) for the registers FG and EC.

The divided clock is delayed by the delay line IF to drive the sequencer circuit formed by the Proms AF and AH and the register AG. The sequencer is controlled by the LS and TT signals, and determines the output data sequence by selecting the Y component from CG, the U/V component from CA, the timing word from CF and the appropriate blanking/sync levels from the Proms CC and DC. This data selection is controlled by the Prom AF.

(b) QUANTEL INTERFACE INPUTS

Quantel digital video from the "Channel 3" input connector on the top rear panel is passed to the card via the 50-way ribbon connector PL1. The data is buffered by KD (Y), KE (U/V) and KF (Key) then clocked through the registers JD, JE and JF to be passed via the 50-way connector PL5 to the Chroma Proc card when selected by the PAL HF.

Quantel digital video from the "Channel 4" input connector on the top rear panel is passed to the card via the 50-way ribbon connector PL2. The data is buffered by KI (Y), KH (U/V) and KG (Key) then clocked through the registers JI, JH and JG to be passed via the 50-way connector PL5 to the Chroma Proc card when selected by the PAL HF.

(c) CONNECTOR DETAILS

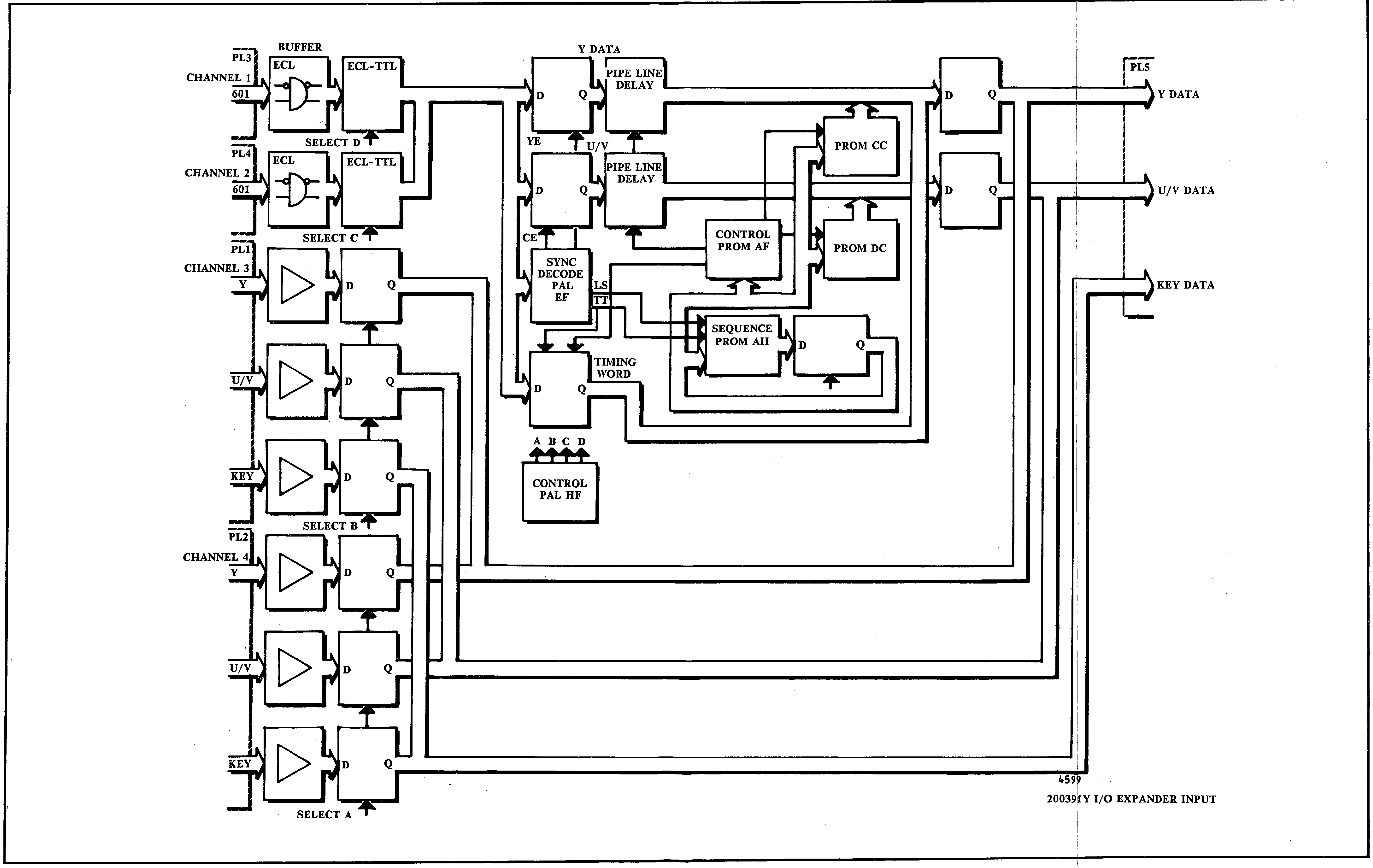
EBU 601 INTERFACE

Pin	Function	
3	+ Data 7 (MSB)	CCIR I/P
4	+ Data 6	CCIR I/P
5	+ Data 5	CCIR I/P
6	+ Data 4	CCIR I/P
7	+ Data 3	CCIR I/P
8	+ Data 2	CCIR I/P
9	+ Data 1	CCIR I/P
10	+ Data 0	CCIR I/P
11		
12		
1	+ Clock	CCIR I/P
2	System Ground	
13	Chassis Ground	
16	- Data 7 (MSB)	CCIR I/P
17	- Data 6	CCIR I/P
18	- Data 5	CCIR I/P
19	- Data 4	CCIR I/P
20	- Data 3	CCIR I/P
21	- Data 2	CCIR I/P
22	- Data 1	CCIR I/P
23	- Data 0	CCIR I/P
24		
25		
14	- Clock	CCIR I/P
15	System Ground	

QUANTEL INTERFACE

Pin	Function
1	Y IN 0H
3	Y IN 1H
5	Y IN 2H
7	Y IN 3H
9	Y IN 4H
11	Y IN 5H
13	Y IN 6H
15	Y IN 7H
17	U/V IN 0H
19	U/V IN 1H
21	U/V IN 2H
23	U/V IN 3H
25	U/V IN 4H
27	U/V IN 5H
29	U/V IN 6H
31	U/V IN 7H
33	KEY IN 0H
35	KEY IN 1H
37	KEY IN 2H
39	KEY IN 3H
41	KEY IN 4H
43	KEY IN 5H
45	KEY IN 6H
47	KEY IN 7H
49	CLOCK IN

(5,4C)
FIGURE 5.4.1 200391YC I/O EXPANDER INPUT BLOCK



(5,4C)

FIGURE 5.4.2 200391YC I/O EXPANDER INPUT LAYOUT

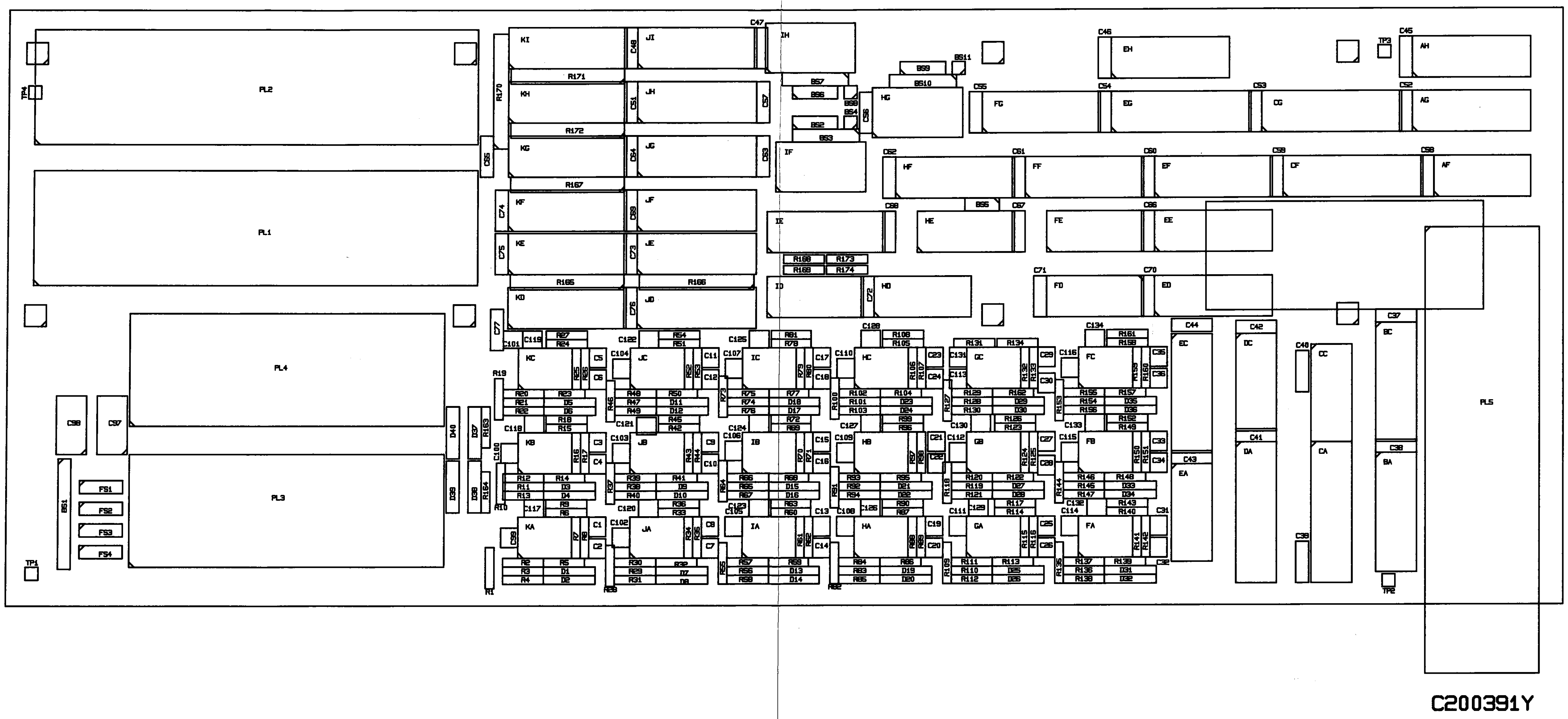
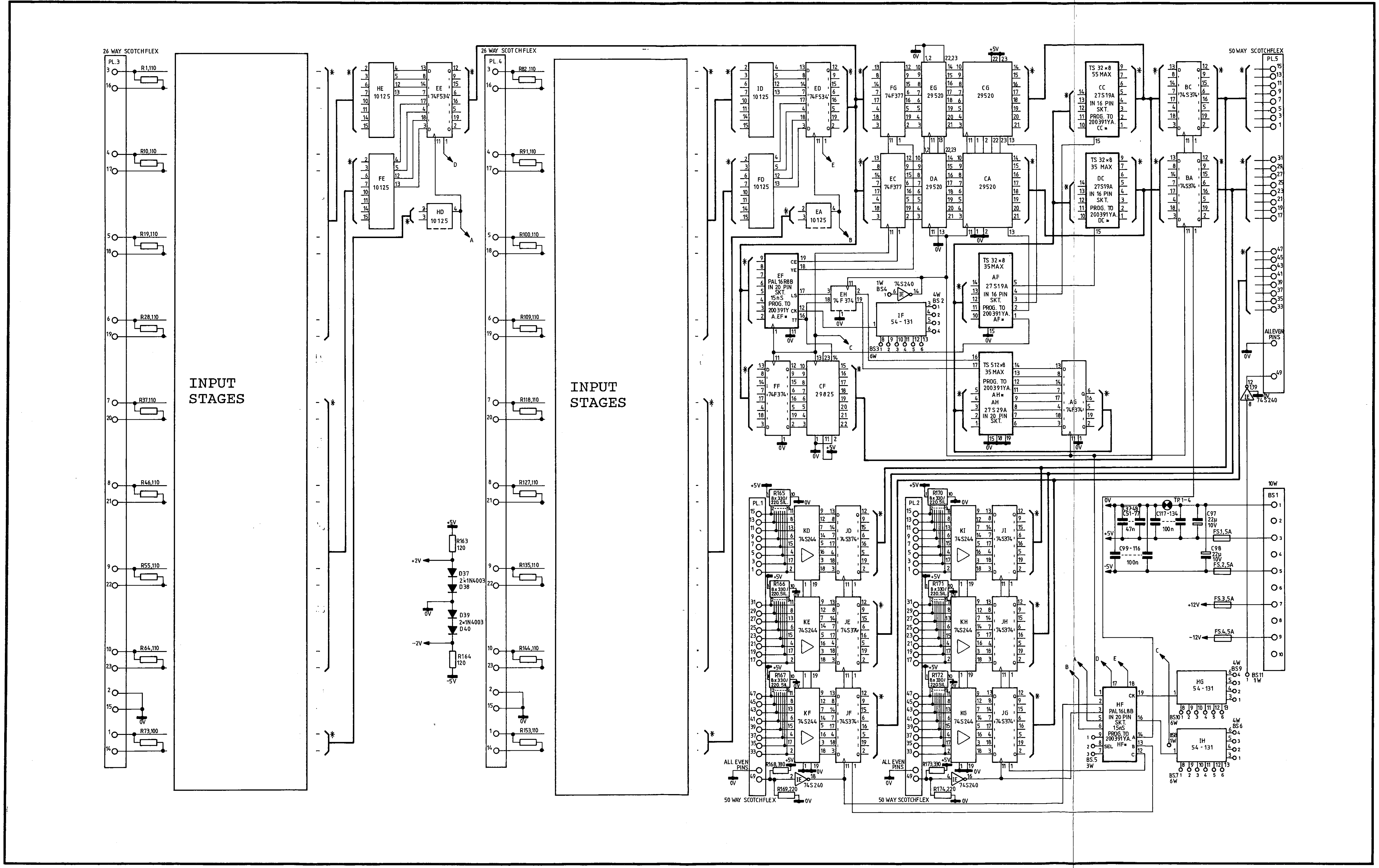


FIGURE 5.4.3 200391YC I/O EXPANDER INPUT CIRCUIT



I/O EXPANDER OUTPUT 2003899B

5:5:1 Function

The function of this card is to provide 4 digital video outputs for the system, 2 EBU 601 digital outputs and 2 Quantel standard digital outputs. The card is mounted in the rear of the Harry crate assembly on the inside of the top rear panel (I/O Panel).

The EBU 601 video data is transmitted as 8-bit complementary pair ECL at 27MHz sample rate. The data is in multiplexed Y, U and V form providing 4:2:2 samples respectively. The Y component has a 13.5MHz sample rate and the U and V samples both have 6.75MHz sample rates. The 601 data is accompanied by a 27MHz clock which is used to de-multiplex the Y, U and V components

The Quantel Standard Video is transmitted as three 8bit TTL data buses at 13.5MHz sample rate. The Y, U/V and Key components are transmitted separately and are each sampled at 13.5MHz. The Quantel Standard data is accompanied by a 13.5MHz clock.

5:5:2 Circuit Description

(a) EBU 601 OUTPUTS

The Y data, the multiplexed U/V data and the Key data from the Coder card are buffered by AE, BB and BA then clocked through the registers AF, CB and CA at 13.5MHz sample rate into the four separate output stages.

The Y and U/V data is clocked through the registers BE and CE into the pipe-line registers BC and CC. The delayed data is then clocked through the registers DC and DB, whose outputs are multiplexed together at 27MHz sample rate.

The Multiplexed Y/U/V data produced at the output of DC and DB is clocked through the register DA into the TTL to ECL converters FA, EA, FB and EB. These provide the EBU 601 ECL outputs for Channel 1 and 2, passed to the rear panel via the 26-way connectors PL3 and PL4.

The sync words embedded in the Luminance data produced by the Coder card are decoded by the PAL EF to produce the timing signals for the sequencer circuit formed by the Prom FE and the register FD. This sequencer controls the insertion, into the 601 sequence, of the EBU 601 sync words held in the Proms ED (Y) and FC (U/V), and the timing word held in the register EE .

The 27MHz clock required for the EBU 601 format is generated by a phase locked oscillator circuit. The oscillator circuit formed by EG and associated components generates a 54MHz clock, which is divided down by the ECL counter FF to provide 27MHz clock (for the EBU 601 outputs) and a 13.5MHz clock (for phase locking). Theses clocks are buffered by GF, then the 13.5MHz clock is passed to the phase comparator GG, where 13.5MHz system clocks are compared. The resulting phase error signal is passed back to the oscillator EG to correct any errors in the 27MHz EBU 601 clock.

(b) QUANTEL INTERFACE OUTPUTS

The Y data, the U/V data and the Key data from the registers AF, CB and CA are clocked through the registers BF/BG (Y), CF/CG (U/V) and DF/DG (Key) to provide the Quantel interface outputs for Channel 3 and Channel 4. These are passed to the rear panel via the 50-way connectors PL1 and PL2.

(c) CONNECTOR DETAILS

EBU 601 INTERFACE

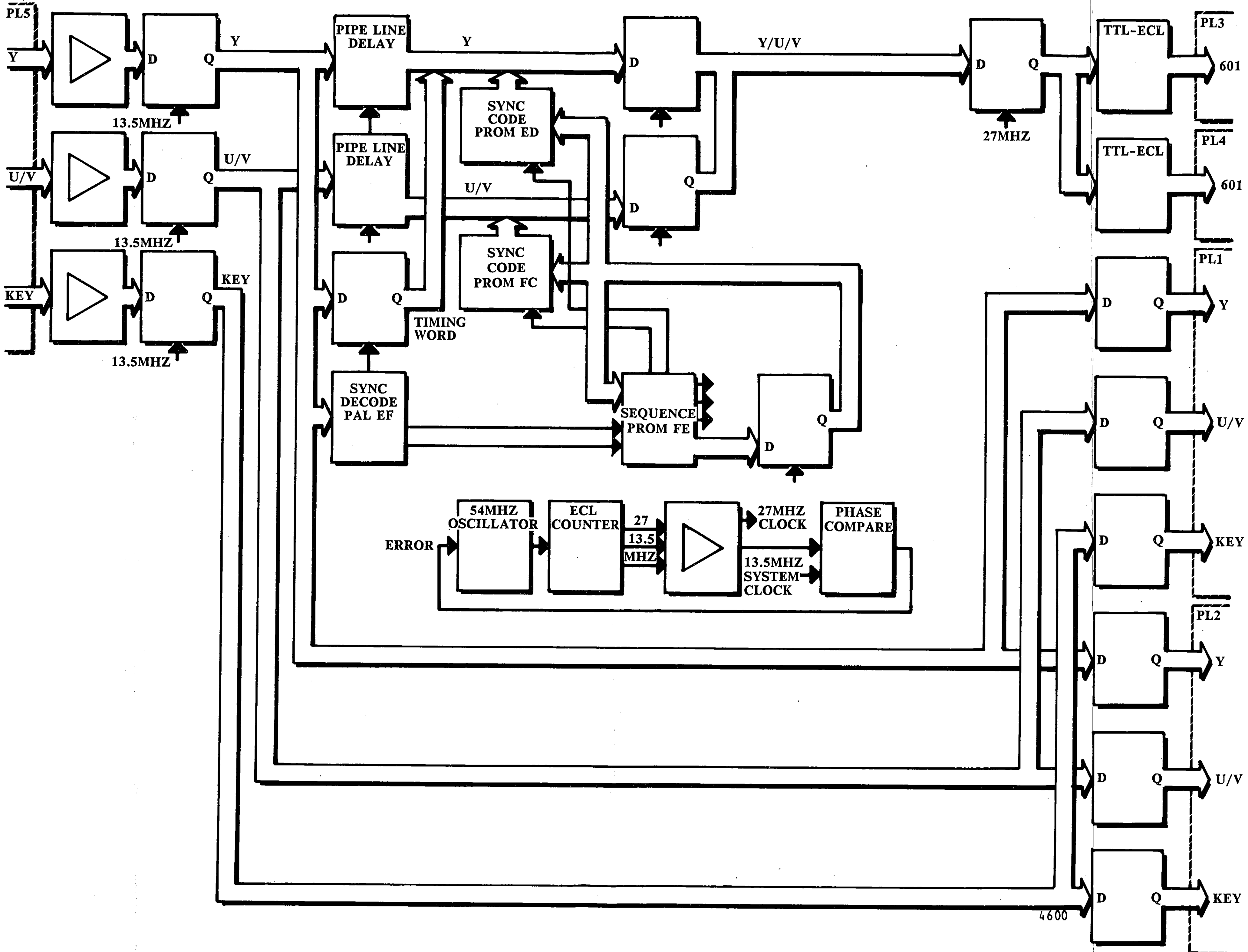
Pin	Function	
3	+ Data 7 (MSB)	CCIR O/P
4	+ Data 6	CCIR O/P
5	+ Data 5	CCIR O/P
6	+ Data 4	CCIR O/P
7	+ Data 3	CCIR O/P
8	+ Data 2	CCIR O/P
9	+ Data 1	CCIR O/P
10	+ Data 0	CCIR O/P
11		
12		
1	+ Clock	CCIR O/P
2	System Ground	
13	Chassis Ground	
16	- Data 7 (MSB)	CCIR O/P
17	- Data 6	CCIR O/P
18	- Data 5	CCIR O/P
19	- Data 4	CCIR O/P
20	- Data 3	CCIR O/P
21	- Data 2	CCIR O/P
22	- Data 1	CCIR O/P
23	- Data 0	CCIR O/P
24		
25		
14	- Clock	CCIR O/P
15	System Ground	

QUANTEL INTERFACE

Pin	Function
1	Y IN 0H
3	Y IN 1H
5	Y IN 2H
7	Y IN 3H
9	Y IN 4H
11	Y IN 5H
13	Y IN 6H
15	Y IN 7H
17	U/V IN 0H
19	U/V IN 1H
21	U/V IN 2H
23	U/V IN 3H
25	U/V IN 4H
27	U/V IN 5H
29	U/V IN 6H
31	U/V IN 7H
33	KEY IN 0H
35	KEY IN 1H
37	KEY IN 2H
39	KEY IN 3H
41	KEY IN 4H
43	KEY IN 5H
45	KEY IN 6H
47	KEY IN 7H
49	CLOCK OUT

(5,5B)

FIGURE 5.5.1 2003899B I/O EXPANDER OUTPUT BLOCK



2003899 I/O EXPANDER OUTPUT

(5,5B)

FIGURE 5.5.2 2003899B I/O EXPANDER OUTPUT LAYOUT

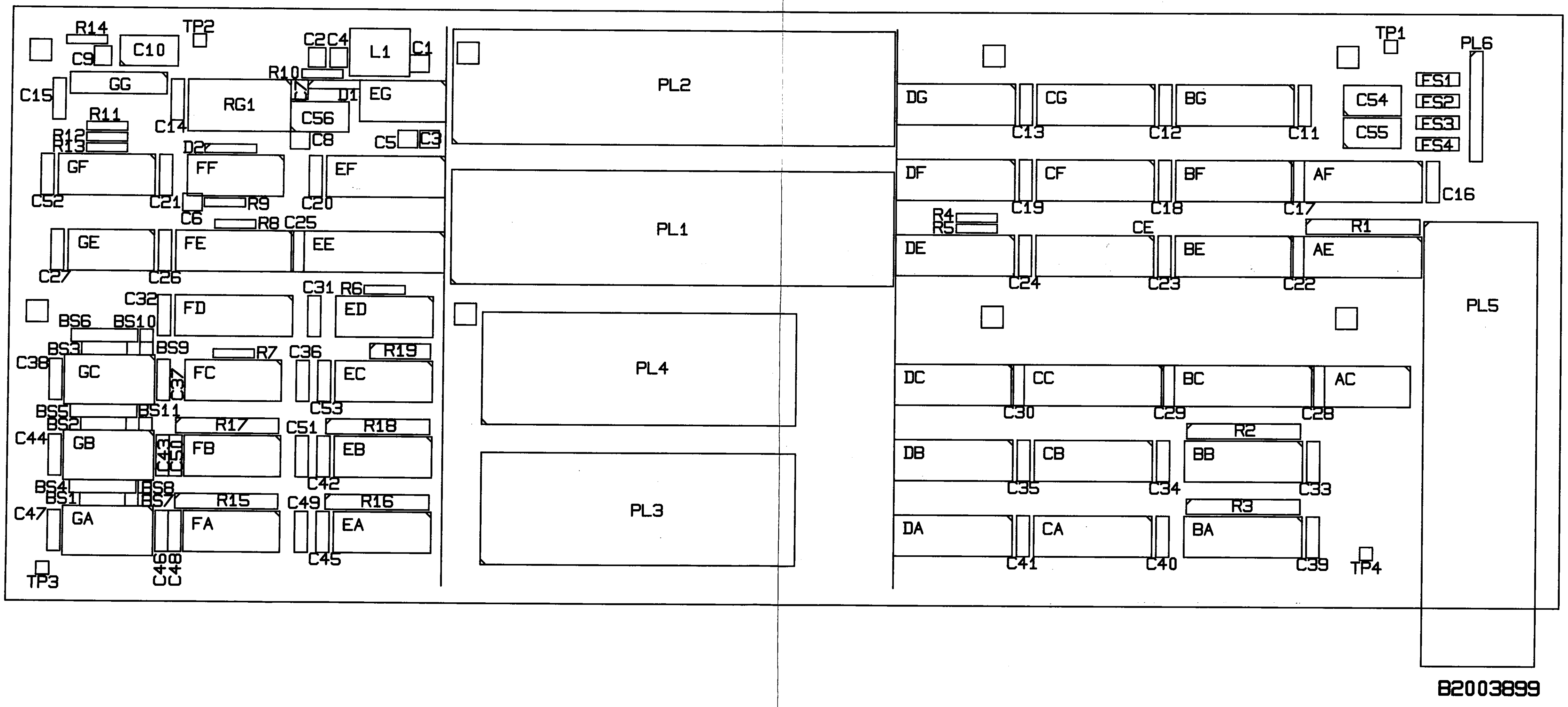
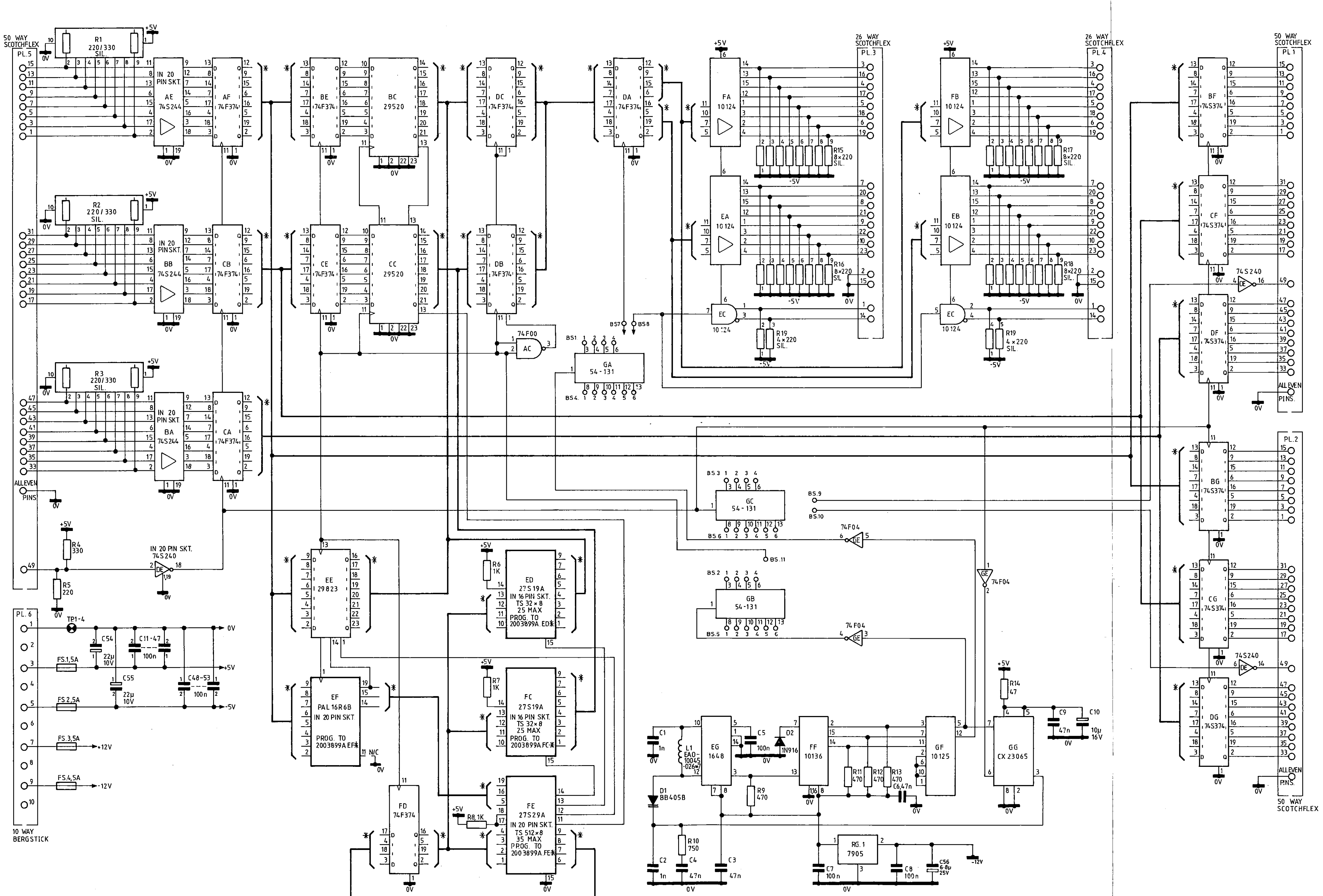


FIGURE 5.5.3 2003899B I/O EXPANDER OUTPUT CIRCUIT



IC. POWER CONNECTIONS.

TYPE	0V	+5V
14 PIN DIL	7	14
16 PIN DIL	8	16
20 PIN DIL	10	20
24 PIN DIL	12	24

TYPE	-5V	0V	+5V
10124	8	16	9
10125	8	16	9

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GLOSSARY OF ABBREVIATIONS

ADC - Analogue Digital Converter
BT - Battery
CAS - Column Address Strobe
CHR - Chrominance
CHROMA - Chrominance
CIO - Computer Input Output
COMP - Computer
CPU - Central Processor Unit
CRC - Circle Redundancy Check
DAC - Digital Analogue Converter
DCR - Digital Cel Recorder
DEMUX - Demultiplexer
DIL - Dual in Line
DMA - Direct Memory Address
ECL - Emitter Coupled Logic
FIFO - First In First Out
FLT - Filter
GND - Ground
HEX - Hexadecimal
HF - High Frequency
IC - Integrated Circuit
I/F - Interface
I/P Input
LDS - Lower Data Strobe
LED - Light Emitting Diode
LF - Low Frequency
LSB - Least Significant Bit
LTC - Longitudinal Time Code
LUMA - Luminance
MSB - Most Significant Bit
MUX - Multiplexer
NTSC - National Television Standards Committee
O/P - Output
PAL - Phase Alternate Line
PCB - Printed Circuit Board
PK - Peak
PROC - Processor
PROM - Programed Read Only Memory
PSU - Power Supply Unit
PTD - Parallel Transfer Drive
RAM - Random Access Memory
RAS - Row Address Strobe
RFI - Radio Frequency Interference
RGB - Component Video
SCSI - Small Computers System Interface
SDLC - Synchronous Data Link Control
SMD - Serial Mode Data
SW - Switch
SYNC - Synchronizing Pulses

GLOSSARY OF ABBREVIATIONS

TP - Test Point
TR - Transistor
TTL - Transistor Transistor Logic
UDS - Upper Data Strobe
U/V - Mulitplexed U and V
VC - Variable Capacitor
VDU - Visual Display Unit
VIA - Virtual Interface Adapter
VID - Video
VITC - Vertical Internal Time Code
VR - Variable Resistor
YUV - Component Video
ZD - Zener Diode

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